

# **VDIC NAND Flash Memory**

## **VDNF64G08XS50XX8V25-III USER MANUAL**

**Version : A2**

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# VDIC-NAND Flash Memory

## HIGH-SPEED 3.3V 8G×8bit

### 1. DESCRIPTION

Offered in 8Gx8bit, the VDNF64G08XS50XX8V25-III is a 64G-bit NAND Flash Memory with spare capacity of 64G -bits. The device operates at 3.3V. The I/O pins serve as the ports for address and data input/output as well as command input.

The VDNF64G08XS50XX8V25-III device is stacked with eight chips. The I/O ports and the control pins (ALE,CLE,#WE,#RE) of each chip are connected.

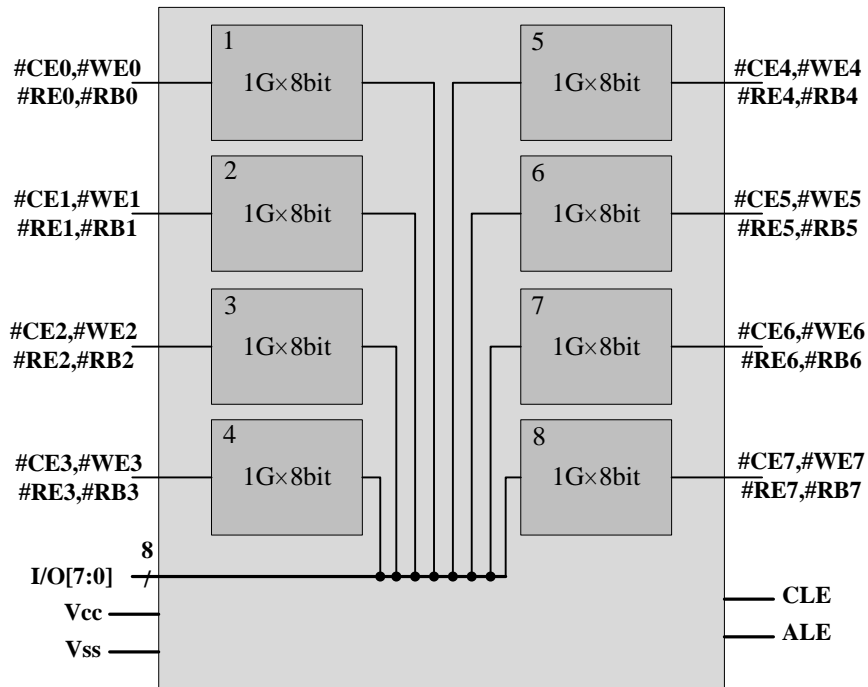
A program operation can be performed in typical 230μs on the (4K+224)Byte page and an erase operation can be performed in typical 700us on a (512K+28K)Byte block. Data in the data register can be read out at 25ns cycle time per Byte.

Every chip has an on-chip write controller which is used to automate all program and erase functions including pulse repetition, where required, and internal verification and margining of data. Even the write-intensive systems can take advantage of the VDNF64G08XS50XX8V25-III's extended reliability of 100K program/erase cycles by providing ECC(Error Correcting Code) with real time mapping-out algorithm. Its NAND cell provides the most cost-effective solution for the solid state application market. The VDNF64G08XS50XX8V25-III is an optimum solution for large nonvolatile storage applications such as solid state data storage and advanced embedded control applications.

## 2. FEATURES

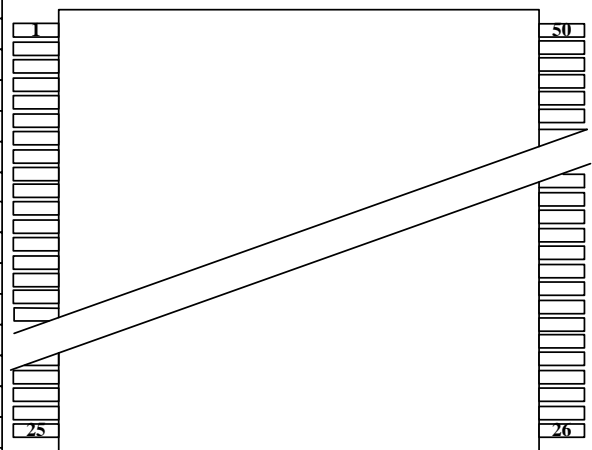
- Voltage Supply
  - 3.3V device: 2.7 ~ 3.6 V
- Organization
  - Memory Cell Array
    - 8chips x (1G +80M)x 8 bit
  - Data Register for each chip
    - (4096 +224) x 8bit
- Automatic Program and Erase
  - Page Program for each chip
    - (4K + 224)Byte
  - Block Erase for each chip
    - (512K +28K)Byte
- Page Read Operation for each chip
  - Page Size
    - (4K + 224)Byte
  - Random Access : 25μs(Max.)
  - Serial Page Access : 25ns(Min.)
- Fast Write Cycle Time
  - Program time : 230μs(Typ.)
  - Block Erase Time : 700us(Typ.)
- Command/Address/Data Multiplexed I/O Port
- Hardware Data Protection
  - Program/Erase Lockout During Power Transitions
- Reliable CMOS Floating-Gate Technology
  - Endurance : 100K Program/Erase Cycles
  - Data Retention : 10 Years
- Command Register Operation
- Intelligent Copy-Back with internal 4bit/540Byte EDC
- Package SOP-50

### 3. BLOCK DIAGRAM



### 4. PIN DESCRIPTIONS– SOP-50

Pin Id	Pin #		Pin Id
#RB7	1	50	#RE7
#RB6	2	49	#RE6
#RB5	3	48	#RE5
#RB4	4	47	#RE4
#R/B3	5	46	#RE3
#R/B2	6	45	I/O7
#R/B1	7	44	I/O6
#R/B0	8	43	I/O5
#RE0	9	42	I/O4
#CE0	10	41	#RE2
#CE1	11	40	#RE1
#CE2	12	39	VCC
VCC	13	38	VCC
VSS	14	37	VSS
#CE3	15	36	VSS
#CE4	16	35	VSS
CLE	17	34	#CE5
ALE	18	33	I/O3
#WE0	19	32	I/O2
#WP	20	31	I/O1
#WE1	21	30	I/O0
#WE2	22	29	#CE7
#WE3	23	28	#CE6
#WE4	24	27	#WE7
#WE5	25	26	#WE6



Name	Function
I/O0~I/O7	<b>DATA INPUTS/OUTPUTS</b> The I/O pins are used to input command, address and data, and to output data during read operations. The I/O pins float to high-z when the chip is deselected or when the outputs are disabled.
CLE	<b>COMMAND LATCH ENABLE</b> The CLE input controls the activating path for commands sent to the command register. When active high, commands are latched into the command register through the I/O ports on the rising edge of the #WE signal.
#CE0 (Chip1)	<b>Chip Enable Input</b> .When #CE <sub>n</sub> is Low, the command input cycle becomes valid in chip n. When #CE <sub>n</sub> is High, all inputs are ignored in chip n.
#CE1 (Chip2)	
#CE2 (Chip3)	
#CE3 (Chip4)	
#CE4 (Chip5)	
#CE5 (Chip6)	
#CE6 (Chip7)	
#CE7 (Chip8)	
ALE	<b>ADDRESS LATCH ENABLE</b> The ALE input controls the activating path for the address to the internal address registers. Addresses are latched on the rising edge of #WE with ALE high.
#RE <sub>n</sub>	<b>READ ENABLE</b> The #RE <sub>n</sub> input is the serial data-out control, and when active , drives the data onto the I/O bus. Data is valid $t_{REA}$ after the falling edge of #RE which also increments the internal column address counter by one.
#WE <sub>n</sub>	<b>WRITE ENABLE</b> The #WE <sub>n</sub> input controls writes to the I/O port. Commands, address and data are latched on the rising edge of the #WE pulse.
#WP	<b>WRITE PROTECT</b> The #WP pin provides inadvertent write/erase protection during power transitions. The internal high voltage generator is reset when the #WP pin is active low.
#R/B0 (Chip1)	<b>READY/BUSY OUTPUT</b> The #R/B <sub>n</sub> output indicates the status of the device operation. When low it indicates that a program, erase or random read operation is in process and returns to high state upon completion. It is an open drain output and does not float to high-z condition when the chip is deselected or when outputs are disabled.
#R/B1 (Chip2)	
#R/B2 (Chip3)	
#R/B3 (Chip4)	
#R/B4 (Chip5)	

Name	Function
#R/B5 (Chip6)	
#R/B6 (Chip7)	
#R/B7 (Chip8)	
VCC	<b>POWER</b> VCC is the power supply for device.
VSS	<b>GROUND</b>

## 5. ELECTRICAL SPECIFICATIONS

### 5.1. Absolute Maximum Ratings

Characteristics	Symbol	Maximum ratings	Unit
Voltage on V <sub>CC</sub> supply relative to V <sub>SS</sub>	V <sub>CC</sub>	-0.6 to +4.6	V
Voltage on any pin relative to V <sub>SS</sub>	V <sub>IN</sub>	-0.6 to +4.6	V
Power Dissipation	P <sub>D</sub>	2	W
Operating Temperature Range	T <sub>A</sub>	-55~ +125	°C
Storage Temperature Range	T <sub>STG</sub>	-65 to +150	°C

### 5.2. Recommended DC Operating Conditions

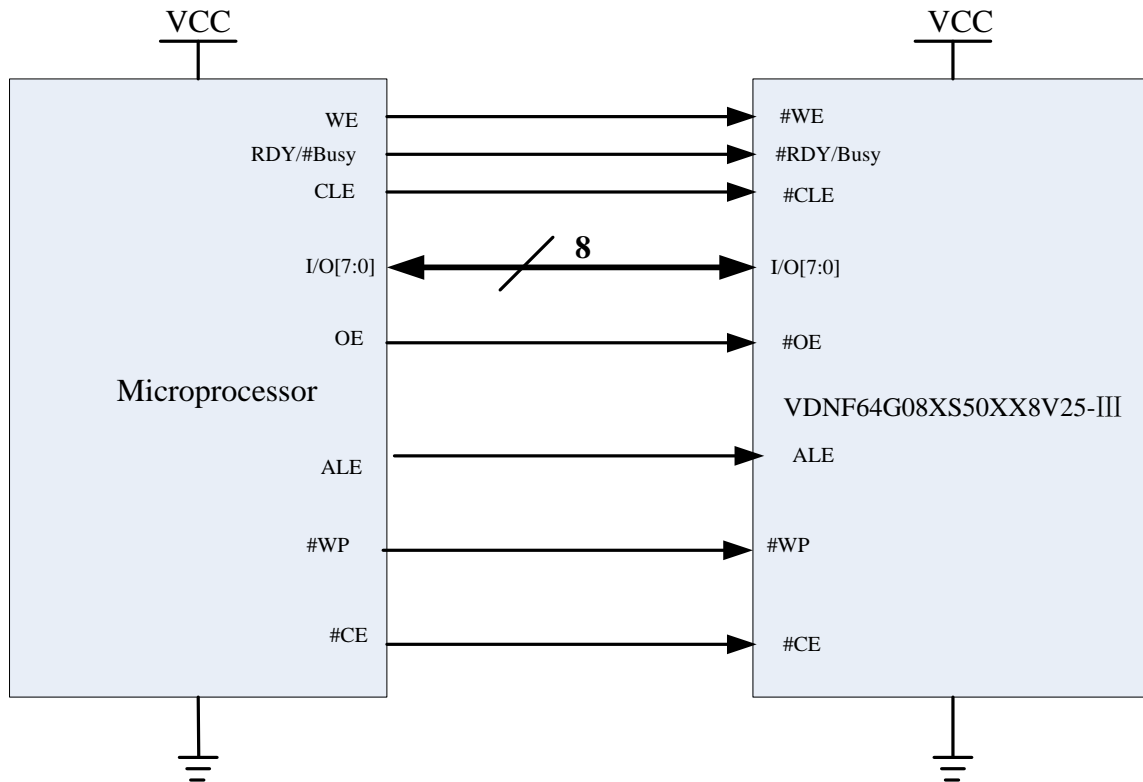
Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V <sub>CC</sub>	2.7	3.3	3.6	V
Input high voltage	V <sub>IH</sub>	V <sub>CC</sub> ×0.8	—	V <sub>CC</sub> +0.3	V
Input low voltage	V <sub>IL</sub>	-0.3	—	V <sub>CC</sub> ×0.2	V

### 5.3. DC And Operating Characteristics

Parameter	Symbol	Test Conditions	Min	Max	Unit
Output voltage low level	V <sub>OL</sub>	V <sub>CC</sub> =2.7V I <sub>OL</sub> =2.1mA	—	0.4	V

Parameter	Symbol	Test Conditions	Min	Max	Unit
Output voltage high level	$V_{OH}$	$V_{CC}=2.7V, I_{OH}=-0.4mA$	2.4	—	V

## 6. Typical Application





## 7. ORDERING INFORMATION

1	2	3	4	5	6	7	8	9	10	11	12	13
<u>VD</u>	<u>NF</u>	<u>64G</u>	<u>08</u>	<u>X</u>	<u>S</u>	<u>50</u>	<u>X</u>	<u>X</u>	<u>8</u>	<u>V</u>	<u>25</u>	<u>III</u>
VDIC												
NAND FLASH												
Capability: 64G bit												
Bus Width: 8 bit												
R= Radiation Data Tested; V= Generic Radiation Data Available												
Package: S=SOP												
50=50 Pin												
Temperature: E=0~70°C;I=-40~85°C;M=-55~125°C;S=Specific												
Quality: E= Sample; B= Industry; M=Military; S= Space												
Stacking Layer:8=8layer												
Power Supply :V=3.3V												
Speed:25= 25ns												
-III=Third Version												

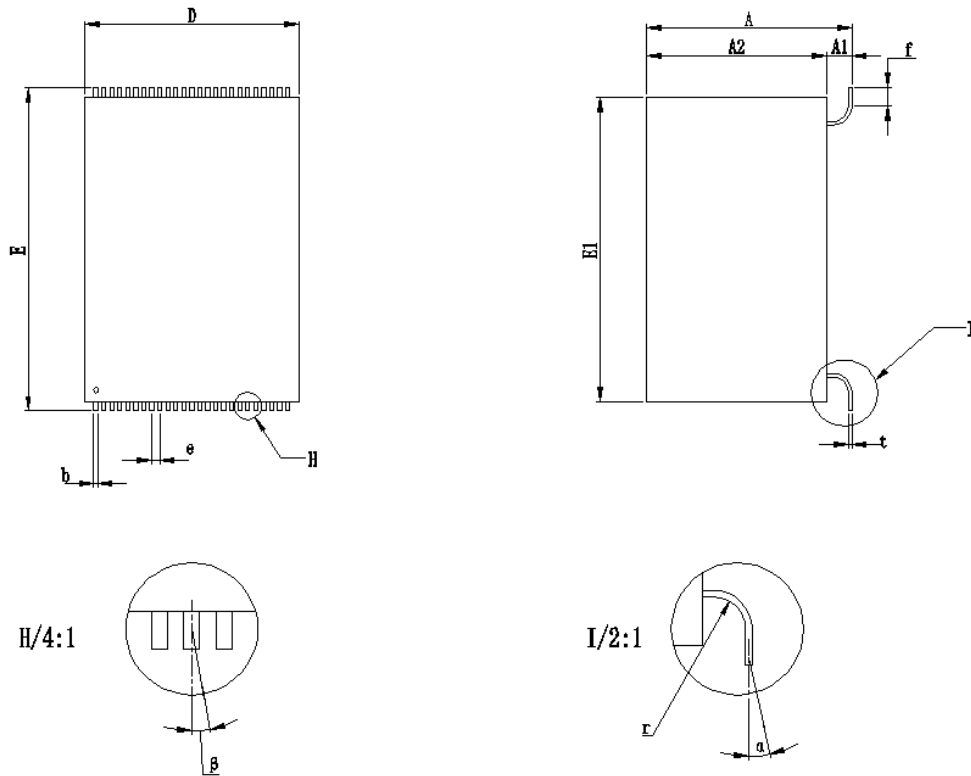
Part Number	Capacity (bit)	Bus Width (bit)	Radiation			Packaging	Temperature ( °C )
			TID <sup>1</sup>	SEL <sup>2</sup>	SEU <sup>3</sup>		
VDNF64G08VS50EE8V25-III	64G	8	-	-	-	SOP50	0 ~ + 70
VDNF64G08VS50IB8V25-III	64G	8	-	-	-	SOP50	-40 ~ + 85
VDNF64G08VS50MB8V25-III	64G	8	-	-	-	SOP50	-55 ~ + 125
VDNF64G08VS50MM8V25-III	64G	8	-	-	-	SOP50	-55 ~ + 125
VDNF64G08RS50MS8V25-III	64G	8	>60	>62.5	1.3	SOP50	-55 ~ + 125

<sup>1</sup> TID: Total Dose (Krad(Si))

<sup>2</sup> SEL: LET Threshold (Mev.cm<sup>2</sup>/mg)

<sup>3</sup> SEU:SEU Threshold (Mev.cm<sup>2</sup>/mg)

## 8. PACKAGE DIMENSIONS



	Min	Max
A	12.30	12.80
A2	11.10	11.50
D	13.30	13.70
E	19.80	20.20
E1	18.80	19.20
f	1.20	
b	0.25	
e	0.50	
r	1.00	
t	0.20	
$\alpha$	$\leq 3^\circ$	
$\beta$	$\leq 3^\circ$	
NOTE : 1. Unit : mm		
2. A1= A - A2		

## 9. REVISION HISTORY

Revision	Date	Description of Change
A0	Nov 21,2016	First Created
A1	Mar 14,2017	Modified the PIN DESCRIPTIONS
A2	Mar 29,2018	Add or reduce chapters