

VDIC NAND Flash Memory

VDNF2T32XP193XX4V25 USER MANUAL

Version : A2

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VDIC-NAND Flash Memory

HIGH-SPEED Asynchronous/Synchronous FALSH

64G×32bit

1. DESCRIPTION

Offered in 64G×32bit, the VDNF2T32XP193XX4V25 is a 2T-bit NAND Flash Memory with spare of 256Gb. The device operates at 3.3V. The I/O pins serve as the ports for address and data input/output as well as command input.

The VDNF2T32XP193XX4V25 device is stacked with eight packages. The operation of each package operates independently. The I/O ports and the control pins (ALE,CLE) of all banks in each package are connected.

Each package devices include an asynchronous data interface for high-performance I/O operations. These devices use a highly multiplexed 8-bit bus (DQx) to transfer commands, address, and data. There are five control signals used to implement the asynchronous data interface: CE#, CLE, ALE, WE#, and RE#. Additional signals control hardware write protection (WP#) and monitor device status (R/B#).

Each package devices additionally includes a synchronous data interface for high-performance I/O operations. When the synchronous interface is active, WE# becomes CLK and RE# becomes W/R#. Data transfers include a bidirectional data strobe (DQS).

A target is the unit of memory accessed by a chip enable signal. A target contains eight NAND Flash dies. A NAND Flash die is the minimum unit that can independently execute commands and report status. A NAND Flash die, in the ONFI specification, is referred to as a logical unit (LUN). For further details, see Device and Array Organization.

2. FEATURES

- Voltage Supply
 - V_{CC} : 2.7 ~ 3.6 V
 - V_{CCQ}: 1.7~1.95V
- Organization
 - Memory Cell Array : 8Packages x 16G x 16bit
 - Page size x8: 8640 bytes (8192 + 448 bytes)
 - Block size: 128 pages (1024K + 56K bytes)
 - Plane size: 2 planes x 2048 blocks per plane
 - Package size: 256Gb: 32,786 blocks
- Synchronous I/O performance
 - Up to synchronous timing mode 5
 - Clock rate: 10ns (DDR)
 - Read/write throughput per pin: 200 MT/s
- Asynchronous I/O performance
 - Up to asynchronous timing mode 5
 - t RC/ t WC: 20ns (MIN)
 - Read/write throughput per pin: 50 MT/s
- Array performance
 - Read page: 35μs (MAX)
 - Program page: 350μs (TYP)
 - Erase block: 1.5ms (TYP)
- RESET (FFh) required as first command after power-on
- Reliability
 - Endurance: 60,000 PROGRAM/ERASE cycles
- Data strobe (DQS) signals provide a hardware method for synchronizing data DQ in the synchronous Interface
- Package PGA193

3. BLOCK DIAGRAM

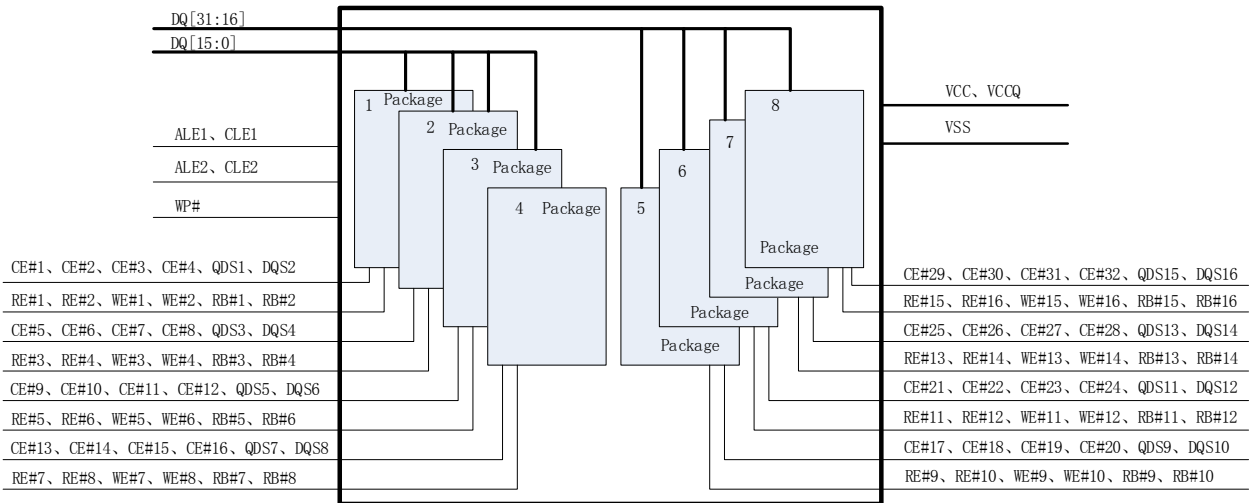


Figure 1:Block Diagram

4. DEVICE ORGANIZATION

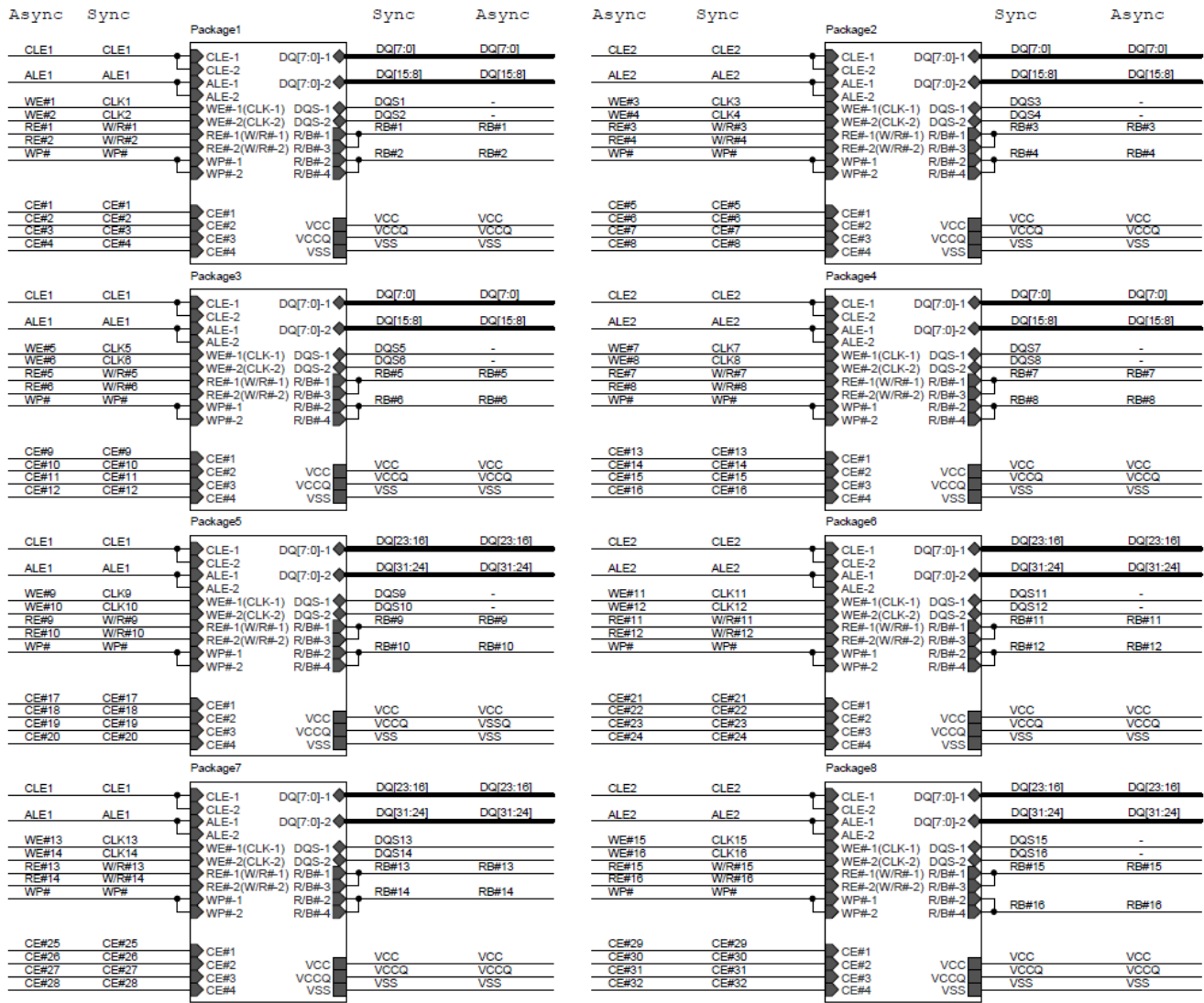


Figure 2:Device Organization

5. PIN DESCRIPTIONS– PGA-193

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
A	WP#	CE#3	DQ8	VSS	DQ24	DQ10	DQ18	CE#18	CE#9	RB#2	RB#14	RB#9	DQ21	DQ7	DQ31	CE#7	
B	CE#11	CE#19	CE#27	VSS	DQ0	DQ26	CE#2	CE#26	CE#17	RB#6	RB#1	RB#13	DQ13	DQ23	ALE2	CE#15	
C	CE#4	CE#12	CE#20	VSS	DQ16	DQ2	CE#10	CE#1	CE#25	RB#10	RB#5	DQ5	DQ29	DQ15	CLE2	CE#23	
D	CE#28	ALE1	CLE1	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	CE#31	
E	VCC	VCC	VCC	VCC	VSS								VSS	VSS	CE#16	CE#8	
F	VCC	VCC	VCC	VCC								VSS	CE#6	CE#32	CE#24		
G	VCCQ	VCCQ	VCCQ	VCCQ								VSS	CE#30	CE#22	CE#14		
H	DQ25	DQ9	DQ27	VSS								VSS	CE#21	CE#13	CE#5		
J	DQ11	DQ17	DQ1	VSS								VSS	RB#8	RB#4	CE#29		
K	DQ19	DQ3	DQS14	VSS								VSS	RB#3	RB#16	RB#12		
L	DQS10	DQS6	DQS2	VSS								VSS	RB#15	RB#11	RB#7		
M	DQS13	DQS9	DQS5	VSS								VSS	VSS	VSS	VSS		
N	DQS1	RE#13	RE#9	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	
P	RE#5	RE#6	WE#2	WE#14	WE#9	DQ28	DQ14	DQ22	DQS12	DQS7	WE#4	WE#16	WE#11	RE#16	VSS	VSS	
R	RE#1	RE#10	WE#6	WE#1	WE#13	DQ4	DQ30	DQS4	DQS16	DQS11	WE#8	WE#3	WE#15	RE#4	RE#8	RE#12	
T	RE#2	RE#14	WE#10	WE#5	DQ12	DQ20	DQ6	DQS8	DQS3	DQS15	WE#12	WE#7	RE#3	RE#7	RE#11	RE#15	

TOP VIEW

Figure 3:Signal Assignments

Table 1:Signal Descriptions

Asynchronous signal ¹	Synchronous signal ¹	Type	Function
DQ0~DQ31	DQ0~DQ31	I/O	Data inputs/outputs: The bidirectional I/Os transfer address, data, and command information.
CLE1、CLE2	CLE1、CLE2	Input	Command latch enable: Loads a command from DQx into the command register.
CE#1 ~CE#32	CE#1 ~CE#32	Input	Chip enable: Enables or disables one or more die (LUNs) in a package's target.
ALE1、ALE2	ALE1、ALE2	Input	Address latch enable: Loads an address from DQx into the address register.
RE#1~RE#16	W/R#1~W/R#16	Input	Read enable and write/read: RE# transfers serial data from the NAND Flash to the host system when the asynchronous interface is active. When the synchronous interface is active, W/R# controls the direction of DQx and DQS.
-	DQS1~DQS16	I/O	Data strobe: Provides a synchronous reference for data input and out-put.
WE#1~WE#16	CLK1~CLK16	Input	Write enable and clock: WE# transfers commands, addresses, and serial data from the host system to the NAND Flash when the asynchronous interface is active. When the synchronous interface is

Asynchronous signal ¹	Synchronous signal ¹	Type	Function
			active, CLK latches command and address cycles.
WP#	WP#	Input	Write protect: Enables or disables array PROGRAM and ERASE operations.
RB#1~RB#16	RB#1~RB#16	Output	Ready/busy: An open-drain, active-low output that requires an external pull-up resistor. This signal indicates target array activity.
VCC	VCC	Supply	VCC: Core power supply
VCCQ	VCCQ	Supply	VCCQ: I/O power supply
VSS	VSS	Supply	VSS: Core ground connection

Notes:

1. See Device Organization for detailed signal connections.

6. ELECTRICAL SPECIFICATIONS

6.1. Absolute Maximum Ratings

Table 2: Absolute Maximum Ratings

Characteristics	Symbol	Maximum ratings	Unit
Voltage on VCC supply relative to Vss	V _{CC}	-0.6 to +4.6	V
Voltage on VCCQ supply relative to VssQ	V _{CCQ}	-0.6 to +4.6	
Voltage on any pin relative to Vss	V _{IN}	-0.6 to +4.6	V
Power Dissipation	P _D	2.0	W
Operating Temperature Range	T _{OPR}	-55~ +125	°C
Storage Temperature Range	T _{STG}	-65 to +150	°C

Notes:1. Voltage on any pin relative to V SS

6.2. Recommended DC Operating Conditions

Table 3: Recommended DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
VCC Supply voltage	V _{CC}	2.7	3.3	3.6	V
VCCQ supply voltage	V _{CCQ}	1.7	1.8	1.95	V
Input high voltage	V _{IH}	0.8×V _{CCQ}	—	V _{CCQ} +0.3	V
Input low voltage	V _{IL}	-0.3	—	0.2×V _{CCQ}	V

6.3. DC And Operating Characteristics

Asynchronous Mode

Table 4:DC And Operating Characteristics(Asynchronous Mode)

Parameter	Symbol	Test Conditions	Min	Max	Unit
Output voltage low level	V _{OL}	V _{CC} =3.6V, V _{CCQ} =1.95V, I _{OL} =2.1mA	—	0.39	V
Output voltage high level	V _{OH}	V _{CC} =2.7V,V _{CCQ} =1.7V,I _{OH} = -0.4mA	1.36	—	V

Synchronous Mode

Table 5:DC And Operating Characteristics(Synchronous Mode)

Parameter	Symbol	Test Conditions	Min	Max	Unit
Output voltage low level	V _{OL}	V _{CC} =3.6V, V _{CCQ} =1.95V, I _{OL} =2.1mA	—	0.39	V
Output voltage high level	V _{OH}	V _{CC} =2.7V,V _{CCQ} =1.7V,I _{OH} = -0.4mA	1.36	—	V

7. TYPICAL APPLICATION

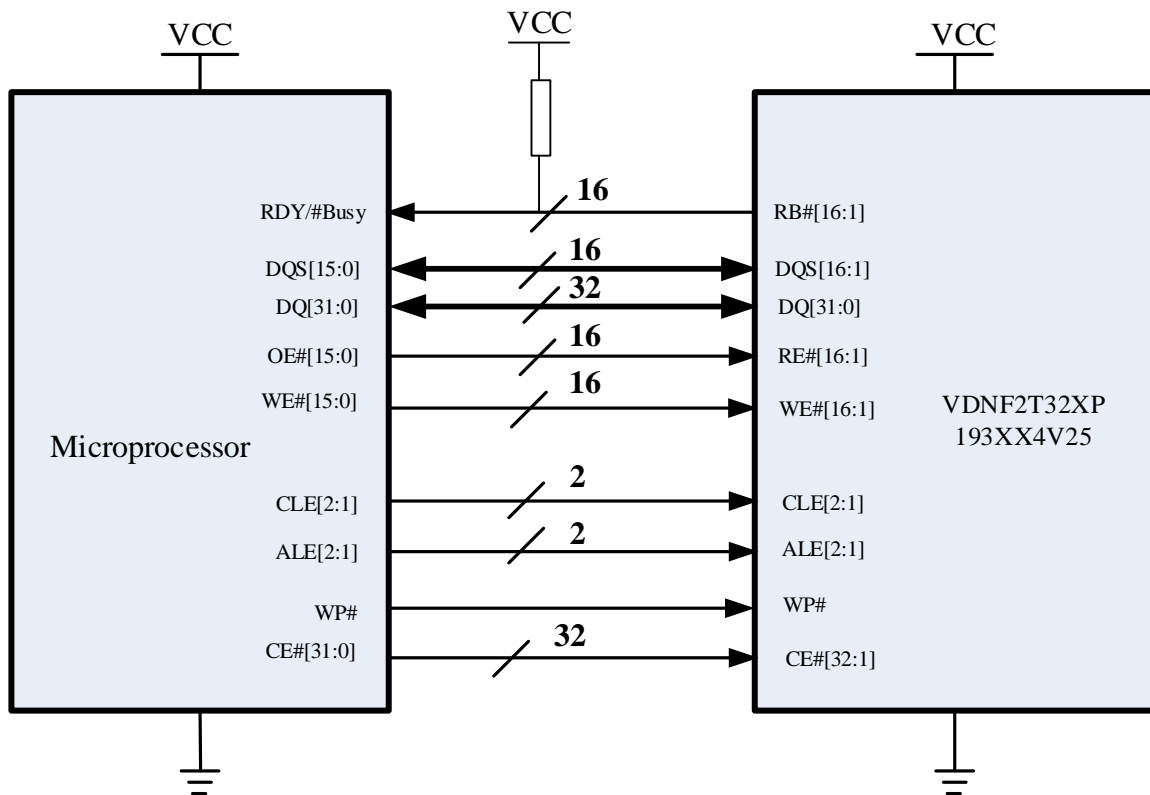


Figure 4:Typical Application

Table 6: Recommended Signal Combination

Group	Signal Combination								WP#
1	CE#1	DQ[7:0]	CLE1	ALE1	DQS1	WE#1	RE#1	RB#1	
	CE#2	DQ[15: 8]			DQS2	WE#2	RE#2	RB#2	
	CE#17	DQ[23:16]			DQS9	WE#9	RE#9	RB#9	
	CE#18	DQ[31:24]			DQS10	WE#10	RE#10	RB#10	
2	CE#3	DQ[7:0]	CLE1	ALE1	DQS1	WE#1	RE#1	RB#1	
	CE#4	DQ[15: 8]			DQS2	WE#2	RE#2	RB#2	
	CE#19	DQ[23:16]			DQS9	WE#9	RE#9	RB#9	
	CE#20	DQ[31:24]			DQS10	WE#10	RE#10	RB#10	
3	CE#5	DQ[7:0]	CLE2	ALE2	DQS3	WE#3	RE#3	RB#3	
	CE#6	DQ[15: 8]			DQS4	WE#4	RE#4	RB#4	
	CE#21	DQ[23:16]			DQS11	WE#11	RE#11	RB#11	
	CE#22	DQ[31:24]			DQS12	WE#12	RE#12	RB#12	
4	CE#7	DQ[7:0]	CLE2	ALE2	DQS3	WE#3	RE#3	RB#3	
	CE#8	DQ[15: 8]			DQS4	WE#4	RE#4	RB#4	
	CE#23	DQ[23:16]			DQS11	WE#11	RE#11	RB#11	
	CE#24	DQ[31:24]			DQS12	WE#12	RE#12	RB#12	
5	CE#9	DQ[7:0]	CLE1	ALE1	DQS5	WE#5	RE#5	RB#5	
	CE#10	DQ[15: 8]			DQS6	WE#6	RE#6	RB#6	
	CE#25	DQ[23:16]			DQS13	WE#13	RE#13	RB#13	
	CE#26	DQ[31:24]			DQS14	WE#14	RE#14	RB#14	
6	CE#11	DQ[7:0]	CLE1	ALE1	DQS5	WE#5	RE#5	RB#5	
	CE#12	DQ[15: 8]			DQS6	WE#6	RE#6	RB#6	
	CE#27	DQ[23:16]			DQS13	WE#13	RE#13	RB#13	
	CE#28	DQ[31:24]			DQS14	WE#14	RE#14	RB#14	
7	CE#13	DQ[7:0]	CLE2	ALE2	DQS7	WE#7	RE#7	RB#7	
	CE#14	DQ[15: 8]			DQS8	WE#8	RE#8	RB#8	
	CE#29	DQ[23:16]			DQS15	WE#15	RE#15	RB#15	
	CE#30	DQ[31:24]			DQS16	WE#16	RE#16	RB#16	
8	CE#15	DQ[7:0]	CLE2	ALE2	DQS7	WE#7	RE#7	RB#7	
	CE#16	DQ[15: 8]			DQS8	WE#8	RE#8	RB#8	
	CE#31	DQ[23:16]			DQS15	WE#15	RE#15	RB#15	
	CE#32	DQ[31:24]			DQS16	WE#16	RE#16	RB#16	

8. ORDERING INFORMATION

1	2	3	4	5	6	7	8	9	10	11	12	13
<u>VD</u>	<u>NF</u>	<u>2T</u>	<u>32</u>	<u>X</u>	<u>P</u>	<u>193</u>	<u>X</u>	<u>X</u>	<u>4</u>	<u>V</u>	<u>25</u>	-
VDIC												
NAND FLASH												
Capability: 2T bit												
Bus Width: 32 bit												
R= Radiation Data Tested; V= Generic Radiation Data Available												
Package: P=PGA												
193=193 Pin												
Temperature: E=0~70°C;I=-40~85°C;M=-55~125°C;S=Specific												
Quality: E= Sample; B= Industry; M=Military; S= Space												
Stacking Layer:4=4layer												
Power Supply :V=3.3V												
Speed:25= 25ns												
-I、 -K or blank space=First Version												

Table 6:Part Information

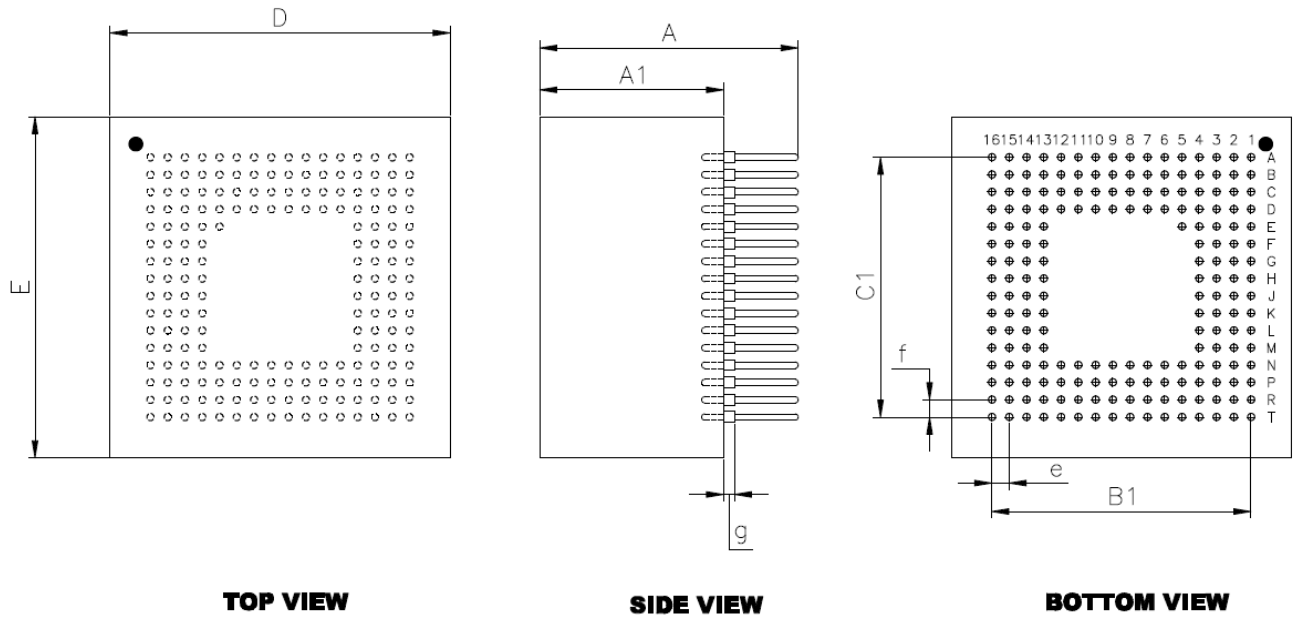
Part Number	Capacity (bit)	Bus Width (bit)	Radiation			Packaging	Temperature (°C)
			TID ¹	SEL ²	SEU ³		
VDNF2T32VP193EE4V25	2T	32	-	-	-	PGA193	0 ~ +70
VDNF2T32VP193IB4V25	2T	32	-	-	-	PGA193	-40 ~ +85
VDNF2T32VP193MM4V25	2T	32	-	-	-	PGA193	-55 ~ +125
VDNF2T32VP193MB4V25	2T	32	-	-	-	PGA193	-55 ~ +125
VDNF2T32RP193MS4V25	2T	32	>60	>62.5	1.3	PGA193	-55 ~ +125

¹ TID: Total Dose (Krad(Si))

² SEL: LET Threshold (Mev.cm²/mg)

³ SEU:SEU Threshold (Mev.cm²/mg)

9. DEVICE DIMENSIONS



	Min	Max
A	18.7	19.3
A1	13.2	13.8
D	25.8	26.2
E	25.8	26.2
B1	e*15	
C1	f*15	
b	0.46±0.05	
e	1.27	
f	1.27	
g	0.8	
NOTE : 1. Unit : mm		

Figure 5:Device Dimensions

10. REVISION HISTORY

Revision	Date	Description of Change
A0	Jun 3,2017	First Created
A1	Mar 27,2018	Add or reduce chapters
A2	May 22,2018	Modified FEATURES