VDIC
NAND FLASH MEMORY

VDNF128G08XS48XX1V25
USER MANUAL

Version :A5

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VDIC-NAND Flash Memory

HIGH-SPEED 3.3V 16G × 8bit

1 Description

The VDNF128G08XS48XX1V25 is a 16G-bit NAND Flash Memory device and operates Voltage at 3.3V. This device contains 1 dies and each die is composed of two banks. Each bank is offered in 64Gx8bit format and can be operated independently and simultaneously by software. The I/O ports of the two banks in each die are connected together. The control pins (ALE,CLE,#WE,#RE) of all banks in the device are connected together.

This hardware interface creates a low pin-count device with a standard pinout that re-mains the same from one density to another, enabling future upgrades to higher densi-ties with no board redesign

The VDNF128G08XS48XX1V25 provides the most cost-effective solution for the solid state application market and is an optimum solution for large nonvolatile storage applications such as solid state data storage and advanced embedded control applications.

2 Features

• Voltage Supply

- 3.3V device: 2.7 ~ 3.6 V

• Organization

- page size x8: 8640 bytes(8192+448 bytes)
- Block size:256 pages(2048K+112K bytes)
- Plane size: 2 Planesx2048 blocks per Plane
- Device size:128G:8192 blocks

• Asynchronous I/O performance

- UP to asynchronous timing mode 5
- ^{t}RC/^{t}WC:25ns（min）

• Array performance

- Read page : 75μs(Max.)
- Program time : 1300μs(Typ.)
- Block Erase Time : 3.8ms(Typ.)

•First block (block address 00h) is valid when ship-ped from Factory.for minimum required ECC,see Error Management

•RESET(FFh) required as first command after power on

• Operation status byte provides software method for detecting

- Operation completion

- Pass/fail condition
- Write-protect status
- Data strobe signals provide a harware method for synchronizing

• Copyback operations supported within the plane from which data is read

• Package :SOP-48

3 Block Diagram

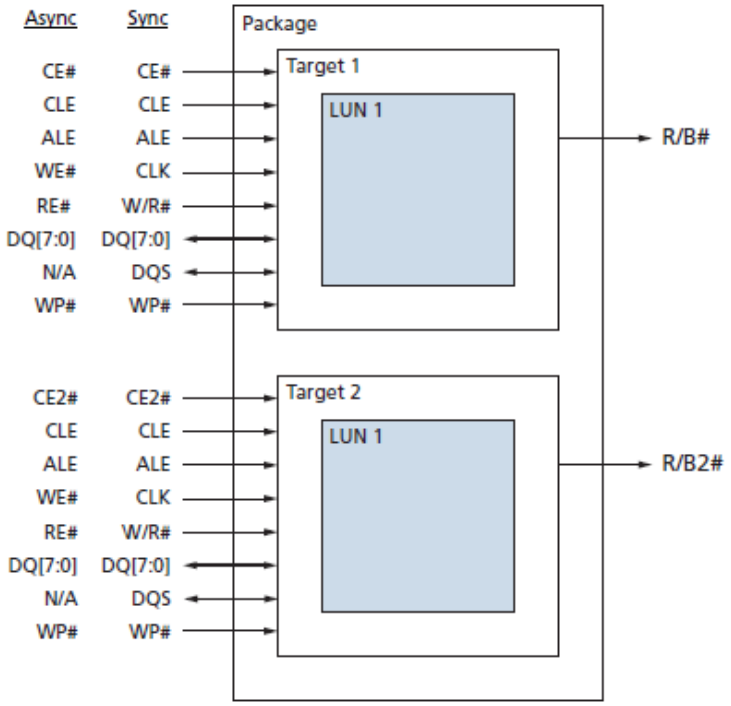

Figure 1 Block diagram

4 Pin Descriptions

Pin Id	Pin #		Pin Id
NC	1	48	**NC**
NC	2	47	**NC**
NC	3	46	**NC**
NC	4	45	**NC**
NC	5	44	**I/O7**
#R/B1	6	43	**I/O6**
#R/B0	7	42	**I/O5**
#RE	8	41	**I/O4**
#CE0	9	40	**NC**
#CE1	10	39	**NC**
NC	11	38	**NC**
VCC	12	37	**VCC**
VSS	13	36	**VSS**
NC	14	35	**NC**
NC	15	34	**NC**
CLE	16	33	**NC**
ALE	17	32	**I/O3**
#WE	18	31	**I/O2**
#WP	19	30	**I/O1**
NC	20	29	**I/O0**
NC	21	28	**NC**
NC	22	27	**NC**
NC	23	26	**NC**
NC	24	25	**NC**

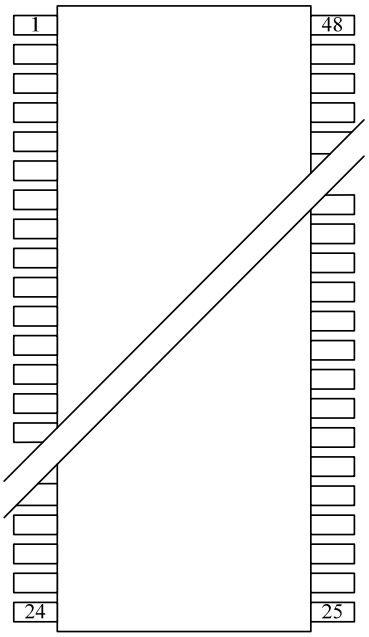

Figure 2 Pin configuration

Table 1 Pin description

Name	Function
I/O0~I/O7	**DATA INPUTS/OUTPUTS** The I/O pins are used to input command, address and data, and to output data during read operations. The I/O pins float to high-z when the chip is deselected or when the outputs are disabled.
CLE	**COMMAND LATCH ENABLE** The CLE input controls the activating path for commands sent to the command register. When active high, commands are latched into the command register through the I/O ports on the rising edge of the #WE signal.
#CE[1:0]	**Bank Enable Input** When #CEn is Low, the command input cycle becomes valid. When #CEn is High, all inputs are ignored.
ALE	**ADDRESS LATCH ENABLE** The ALE input controls the activating path for the address to the internal address registers. Addresses are latched on the rising edge of #WE with ALE high.
#RE	**READ ENABLE** The #RE input is the serial data-out control, and when active，drives the data onto the I/O bus. Data is valid t_{REA} after the falling edge of #RE which also increments the internal column address counter by one.
#WE	**WRITE ENABLE** The #WE input controls writes to the I/O port. Commands, address and data are latched on the rising edge of the #WE pulse.
#WP	**WRITE PROTECT** The #WP pin provides inadvertent write/erase protection during power transitions. The internal high voltage generator is reset when the #WP pin is active low.
#R/B[1:0]	**READY/BUSY OUTPUT** The R/B output indicates the status of the device operation. When low it indicates that a program, erase or random read operation is in process and returns to high state upon completion. It is an open drain output and does not float to high-z condition when the chip is deselected or when outputs are disabled.

Name	Function
V_{CC}	**POWER** V_{CC} is the power supply for device.
V_{SS}	**GROUND**
NC	**NO CONNECTION** Lead is not internally connected.

5 Electrical Specifictions

Stresses greater than those listed can cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not guaranteed. Exposure to absolute maximum rating conditions for extended periods can affect reliability

5.1 Absolute Maximum Ratings

Table 2 Absolute maximum ratings

Characteristics	Symbol	Maximum ratings	Unit
Voltage on V_{CC} supply relative to Vss	V_{CC}	-0.6 ~ +4.6	V
Voltage on any pin relative to Vss	V_{IN}	-0.6 ~ +4.6	V
Power Dissipation	P_D	1.0	W
Operating Temperature Range	T_{OPR}	-55 ~ +125	℃
Storage Temperature Range	T_{STG}	-65 ~ +150	℃

5.2 Recommended DC Operating Conditions

Table 3 Recommended DC operating condition

Parameter	Symbol	Min	Typ	Max	Unit
V_{CC} Supply voltage	V_{CC}	2.7	3.3	3.6	V
Input high voltage	V_{IH}	V_{CC}×0.8	——	V_{CC}+0.3	V
Input low voltage	V_{IL}	-0.3	——	0.2×V_{CC}	V

5.3 DC Characteristics and Operating Conditions

Table 4 DC characteristics

Parameter	Symbol	Test Conditions	Min	Max	Unit
Output voltage low level	V_{OL}	V_{CC}=2.7V，I_{OL}=2.1mA	——	0.4	V
Output voltage high level	V_{OH}	V_{CC}=2.7V，I_{OH}=-0.4mA	2.4	——	V

6 Typical Application

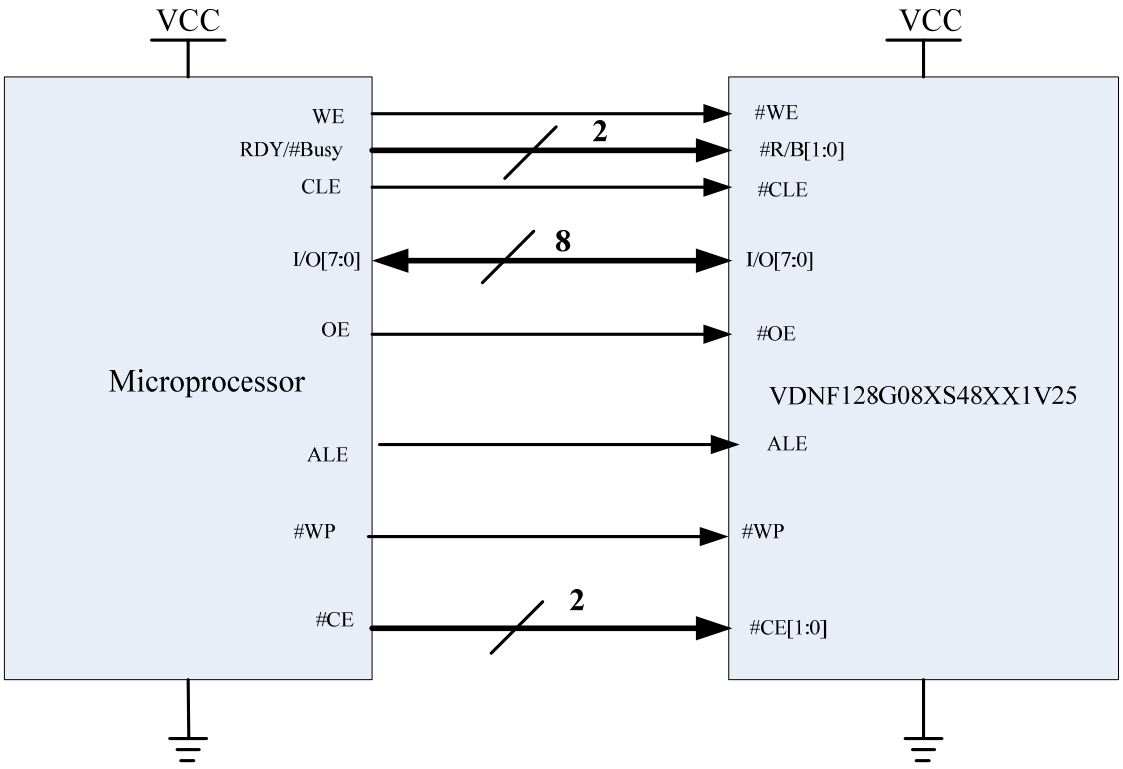

Figure 3 Typical application

7 ORDERING INFORMATION

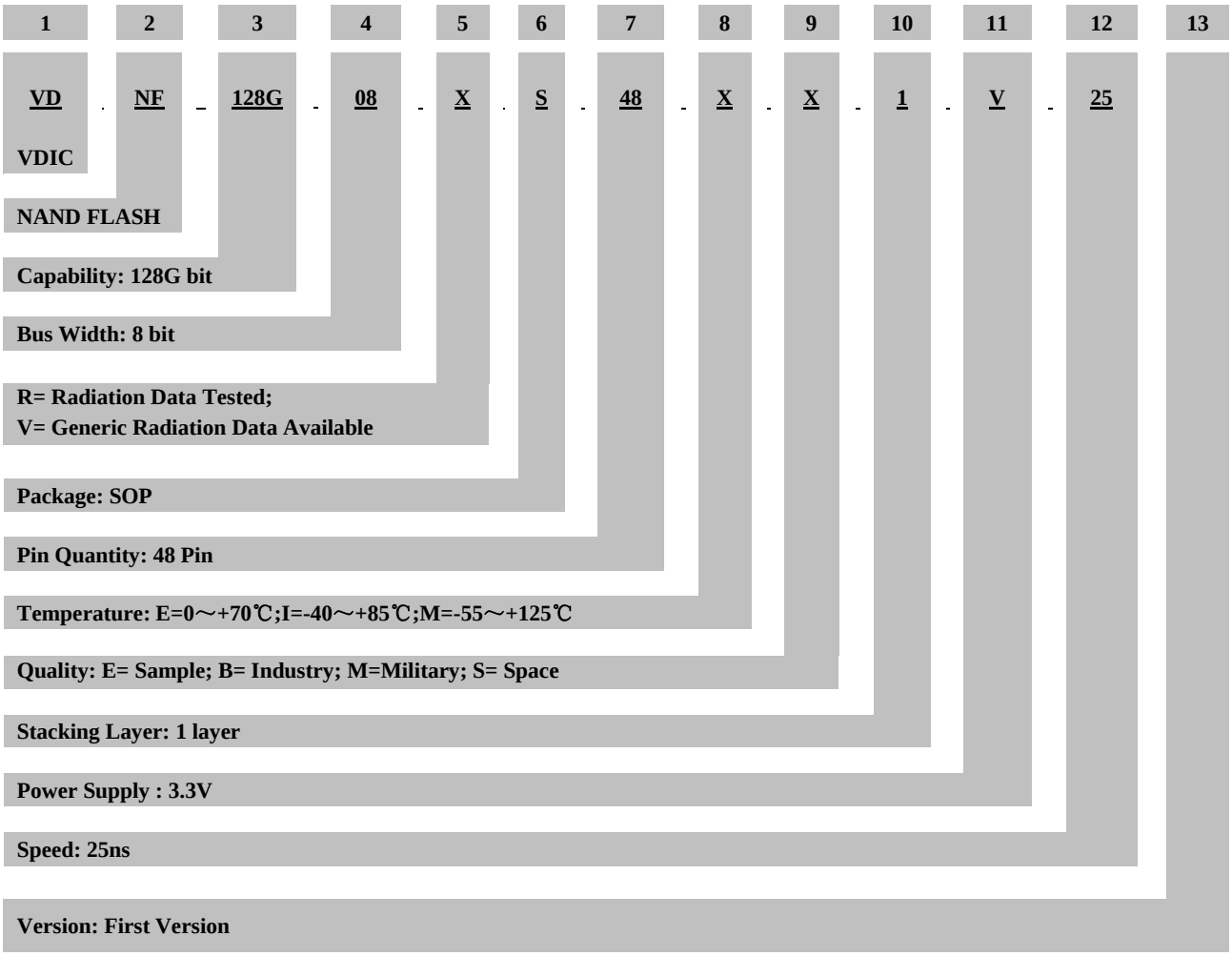

Table 5 Ordering information

Part Number	Capacity (bit)	Bus Width (bit)	Radiation			Packaging	Temperature (℃)
			TID[1]	SEL[2]	SEU[3]		
VDNF128G08VS48EE1V25	128G	8	-	-	-	SOP48	0 ~ +70
VDNF128G08VS48IB1V25	128G	8	-	-	-	SOP48	-40 ~ +85
VDNF128G08VS48MM1V25	128G	8	-	-	-	SOP48	-55 ~ +125
VDNF128G08RS48MS1V25	128G	8	TBD	TBD	TBD	SOP48	-55 ~ +125

[1] TID: Total Dose（Krads(Si)）
[2] SEL: LET Threshold（Mev.cm2/mg）
[3] SEU:SEU Threshold （Mev.cm2/mg）

8 PACKAGE DIMENSIONS

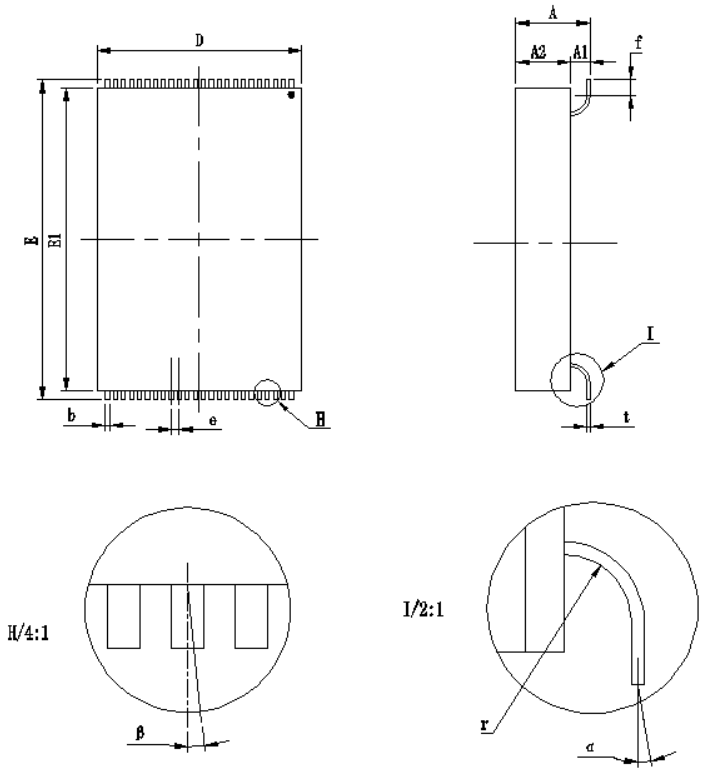

Figure 4 Package dimensions

Table 6 Dimensions information

	Min	Max
A	4.30	5.00
A2	3.10	3.70
D	12.80	13.20
E	19.80	20.20
E1	18.80	19.20
f	1.20	
b	0.25	
e	0.50	
r	1.00	
t	0.20	
α	≤3°	
β	≤3°	
NOTE: 1. Unit: mm 2. A1= A - A2		

9 REVISION HISTORY

Table 7 Revision history

Revision	Date	Description of Change
A0	Nov 3,2015	First Created
A1	Mar 14,2016	Modified the PIN DESCRIPTIONS
A2	Aug 23,2016	Modified the ORDERING INFORMATION
A3	Jan 9,2017	Modified the PACKAGE DIMENSIONS
A4	Oct.25,2017	Changed company's name to Zhuhai Orbita Aerospace Science & Technology Co.，Ltd
A5	Mar 29,2018	Add or reduce chapters