VDIC
NAND FLASH MEMORY

VDNF128G08VS50IB8V25
USER MANUAL

Version : A1

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Contents

VDIC-NAND Flash Memory

HIGH-SPEED 3.3V 16G × 8bit

1 Description

The VDNF128G08VS50IB8V25 is a 128G-bit NAND Flash Memory device and operates Voltage at 3.3V.

This device contains 8 dies and each die is composed of two dies. Each die is offered in 2Gx8bit format and can be operated independently and simultaneously by software. The I/O ports of the two dies in each die are connected together. The control pins (ALE,CLE,#WE,#RE) of all dies in the device are connected together.

This VDNF128G08VS50IB8V25 device include an asynchronous data interface for high-performance I/O operations. These devices use a highly multiplexed 8-bit bus (DQx) to transfer commands, address, and data. There are five control signals used to implement the asynchronous data interface: #CE, CLE, ALE, #WE, and #RE. Additional signals control hardware write protection (#WP) and monitor device status (#R/B).

This hardware interface creates a low pin-count device with a standard pin out that remains the same from one density to another, enabling future upgrades to higher densities with no board redesign

The VDNF128G08VS50IB8V25 provides the most cost-effective solution for the solid state application market and is an optimum solution for large nonvolatile storage applications such as solid state data storage and advanced embedded control applications.

2 Features

• Voltage Supply
  - 3.3V device: 2.7 ~ 3.6 V
• Organization
  - page size x8:4320 bytes(4096+224 bytes)
  - Block size:128 pages(512K+28K bytes)
  - Plane size: 2 Planesx2048 blocks per Plane
  - Device size:128G:32768 block
• Asynchronous I/O performance
  - UP to asynchronous timing mode 5
  - ^{t}RC/^{t}WC:25ns（MIN）
• Array performance
  - Read page : 35μs(Max.)
  - Program time : 350μs(Typ.)
  - Block Erase Time : 1.5ms(Typ.)
• First block (block address 00h) is valid when ship-ped from Factory.for minimum required ECC,see Error Management
• RESET(FFh) required as first command after power on
• Operation status byte provides software method for detecting
  - Operation completion

- Pass/fail condition
- Write-protect status

• Copyback operations supported within the plane from which data is read
• Package
SOP-50

3 Block Diagram

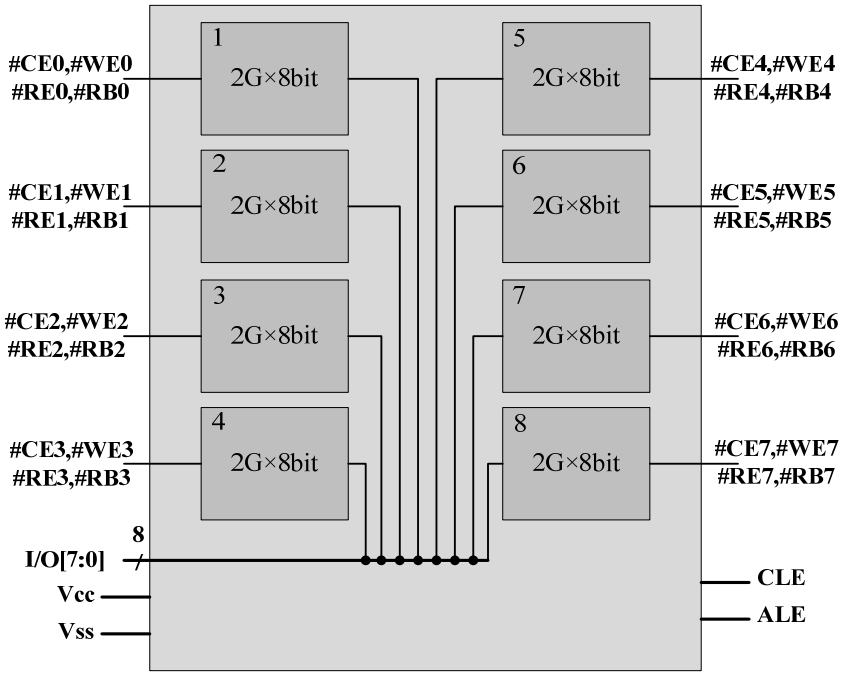

Figure 1 Block diagram

4 Pin Descriptions-sop-50

Pin Id	Pin #		Pin Id
#RB7	1	50	**#RE7**
#RB6	2	49	**#RE6**
#RB5	3	48	**#RE5**
#RB4	4	47	**#RE4**
#RB3	5	46	**#RE3**
#RB2	6	45	**I/O7**
#RB1	7	44	**I/O6**
#RB0	8	43	**I/O5**
#RE0	9	42	**I/O4**
#CE0	10	41	**#RE2**
#CE1	11	40	**#RE1**
#CE2	12	39	**VCC**
VCC	13	38	**VCC**
VSS	14	37	**VSS**
#CE3	15	36	**VSS**
#CE4	16	35	**VSS**
CLE	17	34	**#CE5**
ALE	18	33	**I/O3**
#WE0	19	32	**I/O2**
#WP	20	31	**I/O1**
#WE1	21	30	**I/O0**
#WE2	22	29	**#CE7**
#WE3	23	28	**#CE6**
#WE4	24	27	**#WE7**
#WE5	25	26	**#WE6**

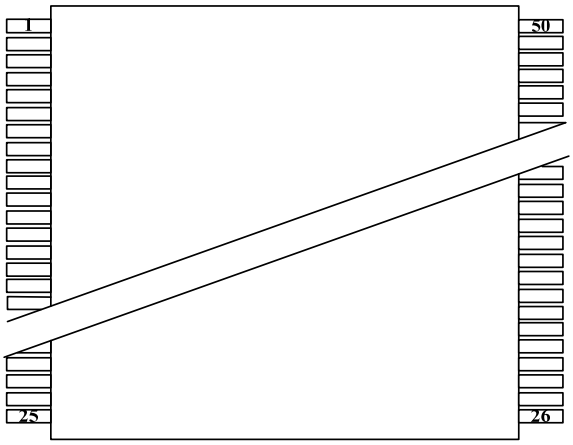

Figure 2 Pin configuration

Table 1: Pin description

Name	Function
DQ0~DQ7	**DATA INPUTS/OUTPUTS** The DQ pins are used to input command, address and data, and to output data during read operations. The DQ pins float to high-z when the chip is deselected or when the outputs are disabled.
CLE	**COMMAND LATCH ENABLE** The CLE input controls the activating path for commands sent to the command register. When active high, commands are latched into the command register through the DQ ports on the rising edge of the #WEn signal.
#CEn	**CHIP ENABLE.** When #CEn is Low, the command input cycle becomes valid. When #CEn is High, all inputs are ignored.
ALE	**ADDRESS LATCH ENABLE** The ALE input controls the activating path for address to the internal address registers. Addresses are latched on the rising edge of #WEn with ALE high.
#REn	**READ ENABLE** The #REn input is the serial data-out control, and when active drives the data onto the DQ bus. Data is valid t_{REA} after the falling edge of #REn which also increments the internal column address counter by one.
#WEn	**WRITE ENABLE** The #WEn input controls writes to the DQ port. Commands, address and data are latched on the rising edge of the #WEn pulse.
#WP	**WRITE PROTECT** The #WP pin provides inadvertent write/erase protection during power transitions. The internal high voltage generator is reset when the #WP pin is active low.
#R/Bn	**READY/BUSY OUTPUT** The #R/Bn output indicates the status of the device operation. When low, it indicates that a program, erase or random read operation is in progress and returns to high state upon completion. It is an open

Name	Function
	drain output and does not float to high-z condition when the chip is deselected or when outputs are disabled.
VCC	**POWER.**
VSS	**GROUND**

5 Electrical Specifications

Stresses greater than those listed can cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not guar-anteed. Exposure to absolute maximum rating conditions for extended periods can affect reliability

5.1 Absolute Maximum Ratings

Table 2:Absolute Maximum Ratings

Characteristics	Symbol	Maximum ratings	Unit
Supply Voltage relative to V_{SS}	V_{CC}	-0.6 ~ +4.6	V
Voltage on any Pin relative to V_{SS}	V_{IN}	-0.6 ~ +4.6	V
Power Dissipation	P_D	2.0	W
Operating Temperature Range	T_{OPR}	-55 ~ +125	℃
Storage Temperature Range	T_{STG}	-65 ~ +150	℃

5.2 Recommended DC Operating Conditions

Table 3:Recommended DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
V_{CC} Supply voltage	V_{CC}	2.7	3.3	3.6	V
Input high voltage	V_{IH}	V_{CC}×0.8	——	V_{CC}+0.3	V
Input low voltage	V_{IL}	-0.3	——	0.2×V_{CC}	V

5.3 DC Characteristics and Operating Conditions

Table 4:DC And Operating Characteristics

Parameter	Symbol	Test Conditions	Min	Max	Unit
Low Level Output Voltage	VOL	Vcc=2.7V，I_{OL}=2.1 mA	-	0.4	V
High Level Output Voltage	VOH	Vcc=2.7V，I_{OH}=-0.4mA	2.4	-	V

6 TYPICAL APPLICATION

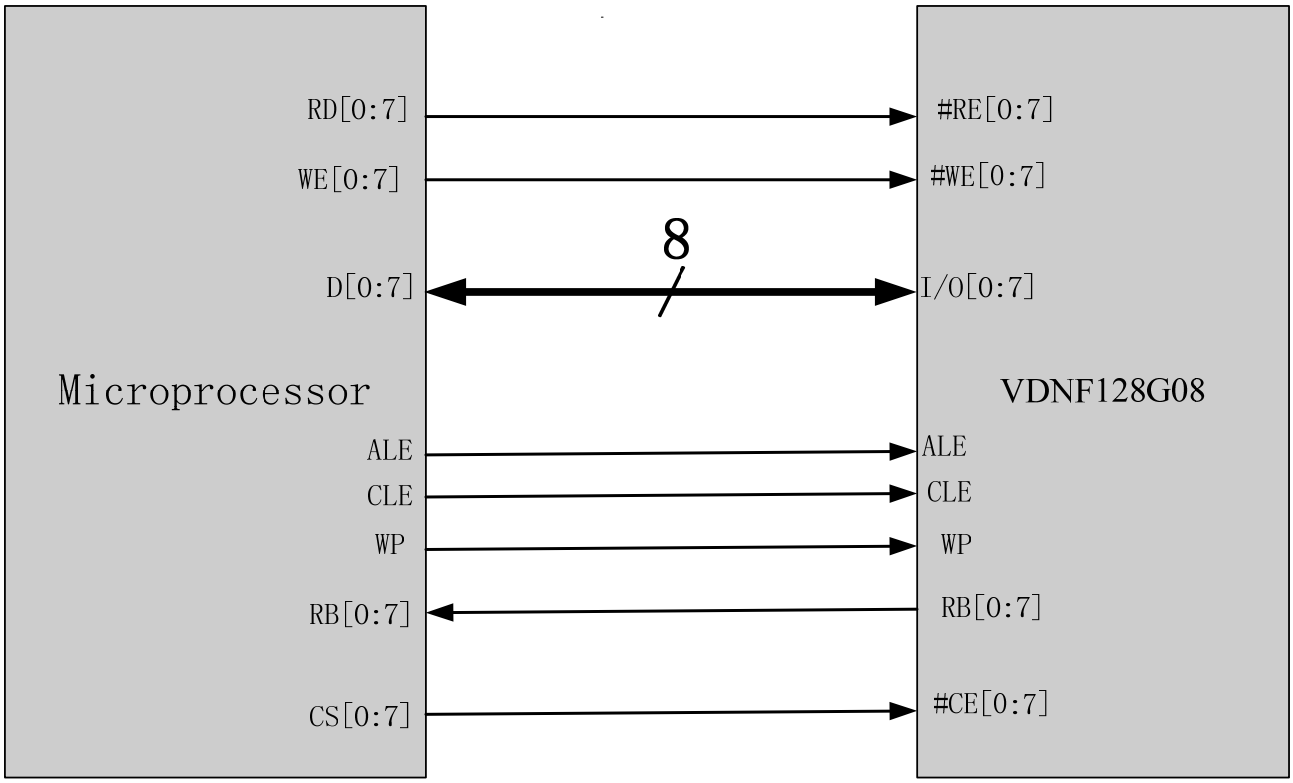

Figure 3 Typical applicatio

7 ORDERING INFORMATION

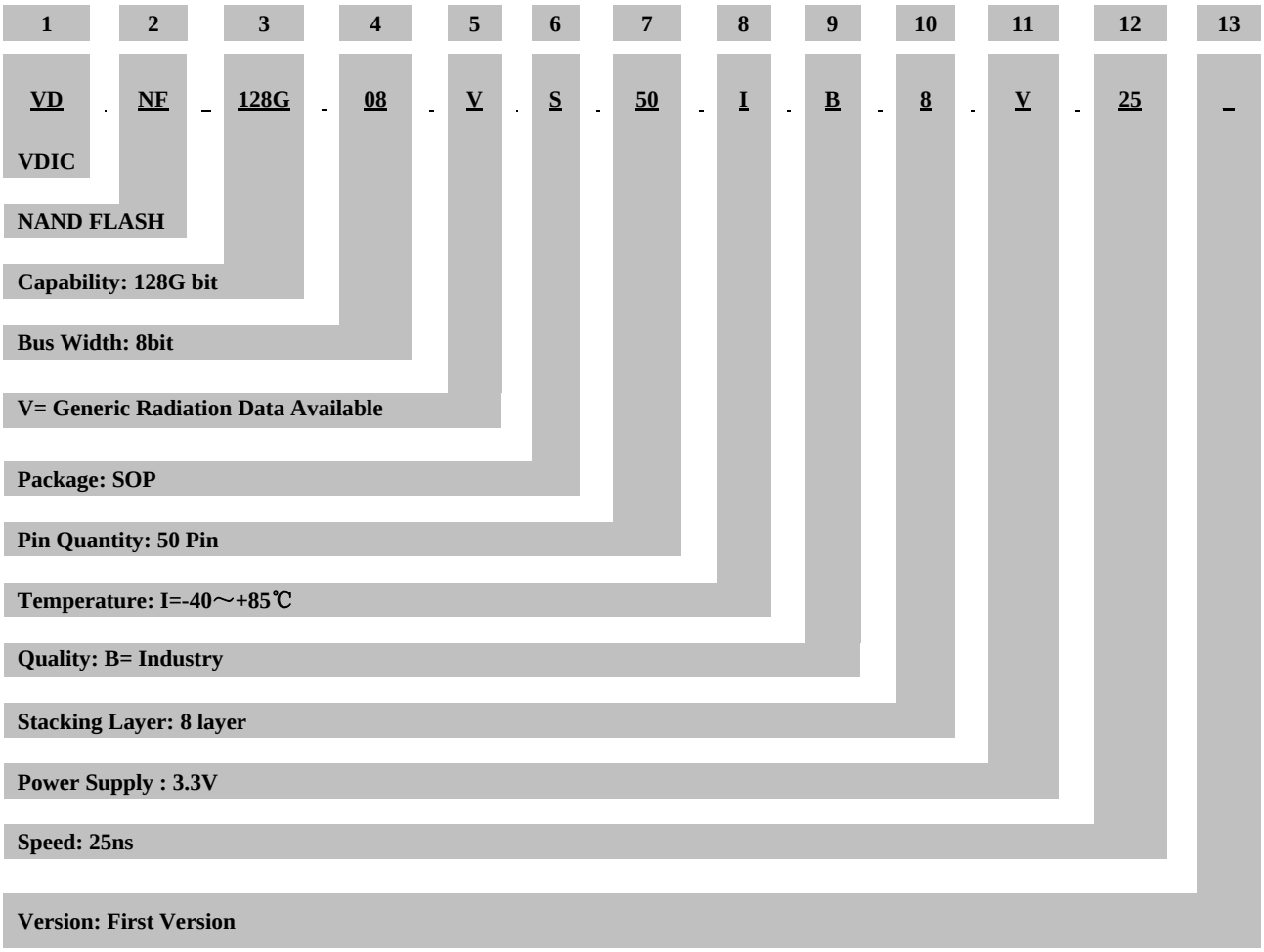

Table 5:Part Information

Part Number	Capacity (bit)	Bus Width (bit)	Radiation			Packaging	Temperature (℃)
			TID[1]	SEL[2]	SEU[3]		
VDNF128G08VS50IB8V25	128G	8	-	-	-	SOP50	-40 ~ +85

[1] TID: Total Dose（Krads(Si)）
[2] SEL: LET Threshold（Mev.cm2/mg）
[3] SEU:SEU Threshold （Mev.cm2/mg）

8 PACKAGE DIMENSIONS

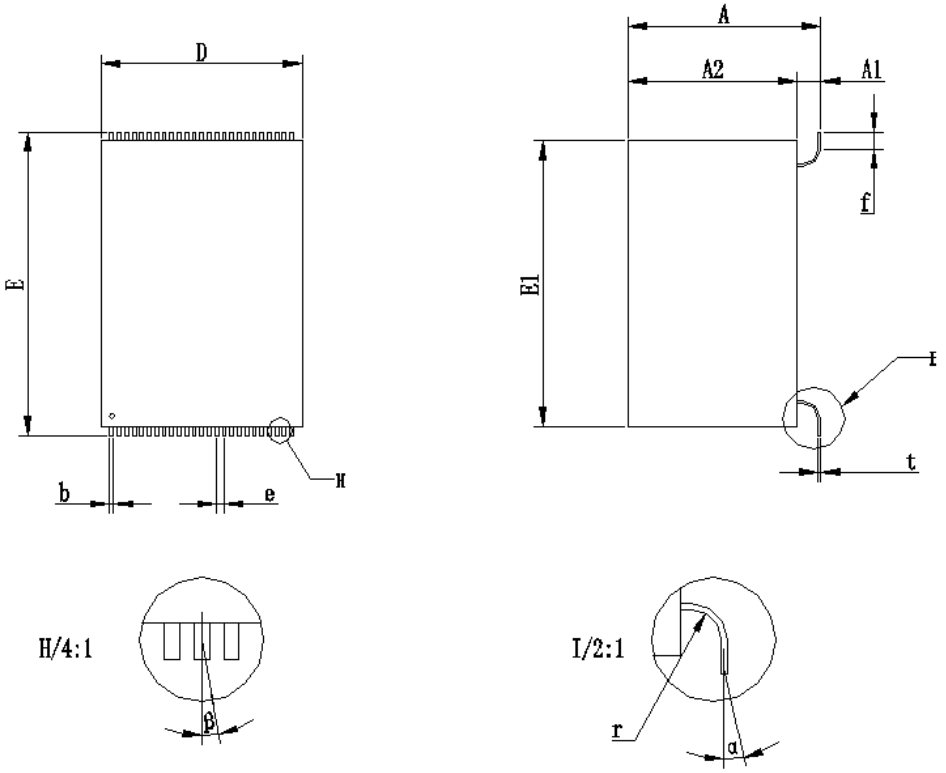

Figure 4 Package dimensions

Table 6 Dimensions information

	Min	Max
A	12.30	12.80
A2	11.10	11.50
D	13.30	13.70
E	19.80	20.20
E1	18.80	19.20
f	1.20	
b	0.25	
e	0.50	
r	1.00	
t	0.20	
α	≤3°	
β	≤3°	
NOTE: 1. Unit: mm 2. A1= A – A2		

9 REVISION HISTORY

Table 7 Revision history

Revision	Date	Description of Change
A0	Nov 25,2017	First Created
A1	Nov 25,2017	Add or reduce the chapters