VDIC
NAND FLASH MEMORY

VDNF64G16XS58XX8V25-Ⅲ
USER MANUAL

Version : A2

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VDIC-NAND Flash Memory

HIGH-SPEED 3.3V 4G×16bit

1. DESCRIPTION

Offered in 4Gx16bit, the VDNF64G16XS58XX8V25-Ⅲ is a 64G-bit NAND Flash Memory with spare capacity of 3584M-bits. The device operates at 3.3V. The I/O pins serve as the ports for address and data input/output as well as command input.

The VDNF64G16XS58XX8V25-Ⅲ device is stacked with eight dies. A program operation can be performed in typical 230μs on the (4K+224)Byte page and an erase operation can be performed in typical 0.7ms on a (512K+28K)Byte block. Data in the data register can be read out at 25ns cycle time per Byte.

Every die has an on-chip write controller which is used to automate all program and erase functions including pulse repetition, where required, and internal verification and margining of data. Even the write-intensive systems can take advantage of the VDNF64G16XS58XX8V25-Ⅲ′s extended reliability of 100K program/erase cycles by providing ECC(Error Correcting Code) with real time mapping-out algorithm.

Its NAND cell provides the most cost-effective solution for the solid state application market. The VDNF64G16XS58XX8V25-Ⅲ is an optimum solution for large nonvolatile storage applications such as solid state data storage and advanced embedded control applications.

2. FEATURES

- Organization
  - Memory Cell Array (1G+56M)bit x 16bit x 4
- Automatic Program and Erase.
  - Page Program : (4K+224) Bytes/Bank
  - Block Erase : (512K+28K) Bytes/Bank
- Single [+2.7;+3.6] V power supply operation
- READ performance
  - Random READ: 25μs (Max.)
  - Serial Access: 25 ns (Min.)
- WRITE performance
  - Program page: 230μs (Typ.)
  - Block Erase: 700μs (Typ.)
- Command/Address/Data Multiplexed I/O Port
- Reliable CMOS Floating-Gate Technology
  - Endurance : 100k Program/Erase Cycles

- Data Retention : 10 Years

- Package SOP-58

3. BLOCK DIAGRAM

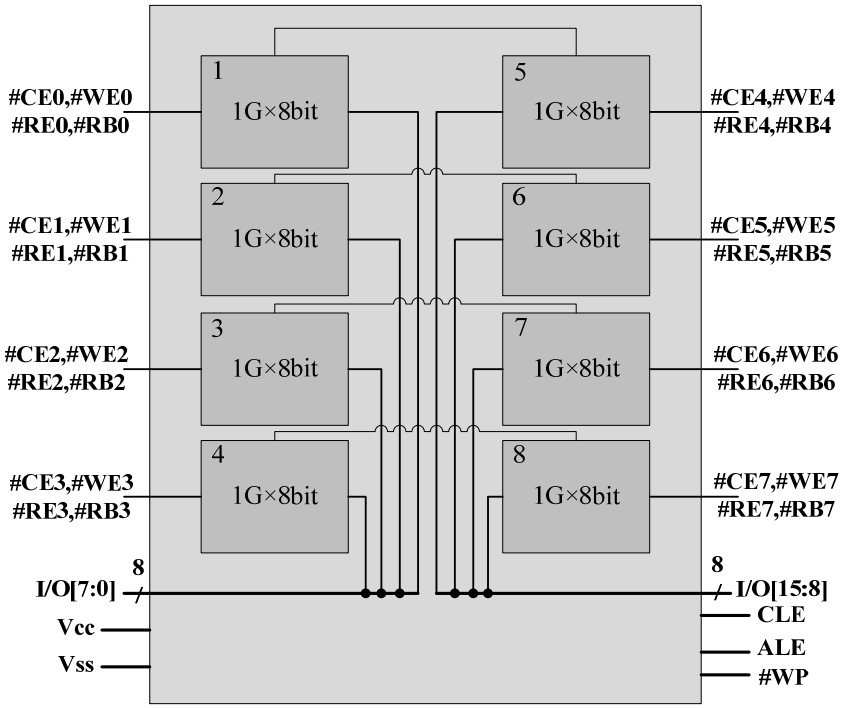

Figure 1 Block diagram

4. PIN DESCRIPTIONS -SOP-58

Pin Id	Pin #		Pin Id
#RE1	1	58	**#RE6**
#RE7	2	57	**#RE5**
#RB7	3	56	**#RE4**
#RB6	4	55	**#RE3**
#RB5	5	54	**#RE2**
#RB4	6	53	**I/O14**
#RB3	7	52	**I/O15**
#RB2	8	51	**I/O7**
#RB1	9	50	**I/O6**
#RB0	10	49	**I/O5**
#RE0	11	48	**I/O4**
#CE0	12	47	**I/O12**
#CE1	13	46	**I/O13**
#CE2	14	45	**NC**
VCC	15	44	**VCC**
VSS	16	43	**VSS**
#CE7	17	42	**NC**
NC	18	41	**I/O10**
CLE	19	40	**I/O11**
ALE	20	39	**I/O3**
#WE0	21	38	**I/O2**
#WP	22	37	**I/O1**
#WE7	23	36	**I/O0**
#WE1	24	35	**I/O8**
#WE2	25	34	**I/O9**
#WE3	26	33	**#CE3**
#WE4	27	32	**#CE4**
#WE5	28	31	**#CE5**
#WE6	29	30	**#CE6**

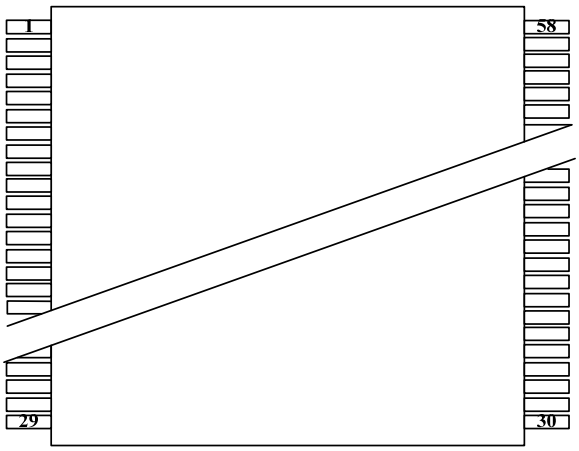

Figure 2 Pin configuration

Table 1: Pin description

Name	Function
I/O0~I/O15	**DATA INPUTS/OUTPUTS** The I/O pins are used to input command, address and data, and to output data during read operations. The I/O pins float to high-z when the chip is deselected or when the outputs are disabled.
CLE	**COMMAND LATCH ENABLE** The CLE input controls the activating path for commands sent to the command register. When active high, commands are latched into the command register through the I/O ports on the rising edge of the #WE signal.
#CE0 (Die1)	**Die Enable Input .**When #CEn is Low, the command input cycle becomes valid. When #CEn is High, all inputs are ignored.
#CE1 (Die2)	
#CE2 (Die3)	
#CE3 (Die4)	
#CE4 (Die5)	
#CE5 (Die6)	
#CE6 (Die7)	
#CE7 (Die8)	

Name	Function
ALE	**ADDRESS LATCH ENABLE** The ALE input controls the activating path for the address to the internal address registers. Addresses are latched on the rising edge of #WE with ALE high.
#REn	**READ ENABLE** The #REn input is the serial data-out control, and when active , drives the data onto the I/O bus. Data is valid t_{REA} after the falling edge of #RE which also increments the internal column address counter by one.
#WEn	**WRITE ENABLE** The #WEn input controls writes to the I/O port. Commands, address and data are latched on the rising edge of the #WE pulse.
#WP	**WRITE PROTECT** The #WP pin provides inadvertent write/erase protection during power transitions. The internal high voltage generator is reset when the #WP pin is active low.
#RB0 (Die1)	**READY/BUSY OUTPUT** The #R/Bn output indicates the status of the device operation. When low it indicates that a program, erase or random read operation is in process and returns to high state upon completion. It is an open drain output and does not float to high-z condition when the chip is deselected or when outputs are disabled.
#RB1 (Die2)	
#RB2 (Die3)	
#RB3 (Die4)	
#RB4 (Die5)	
#RB5 (Die6)	
#RB6 (Die7)	
#RB7 (Die8)	
VCC	**POWER** VCC is the power supply for device.
VSS	**GROUND**

Notes :
1. Connect all V_{CC} and V_{SS} pins of each device to common power supply outputs.
2. Do not leave V_{CC} or V_{SS} disconnected.

5. ELECTRICAL SPECIFICATIONS

5.1 Absolute Maximum Ratings

Table 2:Absolute Maximum Ratings

Characteristics	Symbol	Maximum ratings	Unit
Voltage on VCC supply relative to Vss	V_{CC}	-0.6 ~ +4.6	V
Voltage on any pin relative to Vss	V_{IN}	-0.6 ~ +4.6	V
Power Dissipation	P_D	1.5	W
Operating Temperature Range	T_{OPR}	-55 ~ +125	℃
Storage Temperature Range	T_{STG}	-65 ~ +150	℃

5.2 Recommended DC Operating Conditions

Table 3:Recommended DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	2.7	3.3	3.6	V
Input high voltage	V_{IH}	V_{CC}×0.8	——	V_{CC}+0.3	V
Input low voltage	V_{IL}	-0.3	——	V_{CC}×0.2	V

5.3 DC And Operating Characteristics

Table 4:DC And Operating Characteristics

Parameter	Symbol	Test Conditions	Min	Max	Unit
Output voltage low level	V_{OL}	V_{CC}=2.7V I_{OL} =2.1mA	——	0.4	V
Output voltage high level	V_{OH}	V_{CC}=2.7V,I_{OH}= -0.4mA	2.4	——	V

6. Typical Application

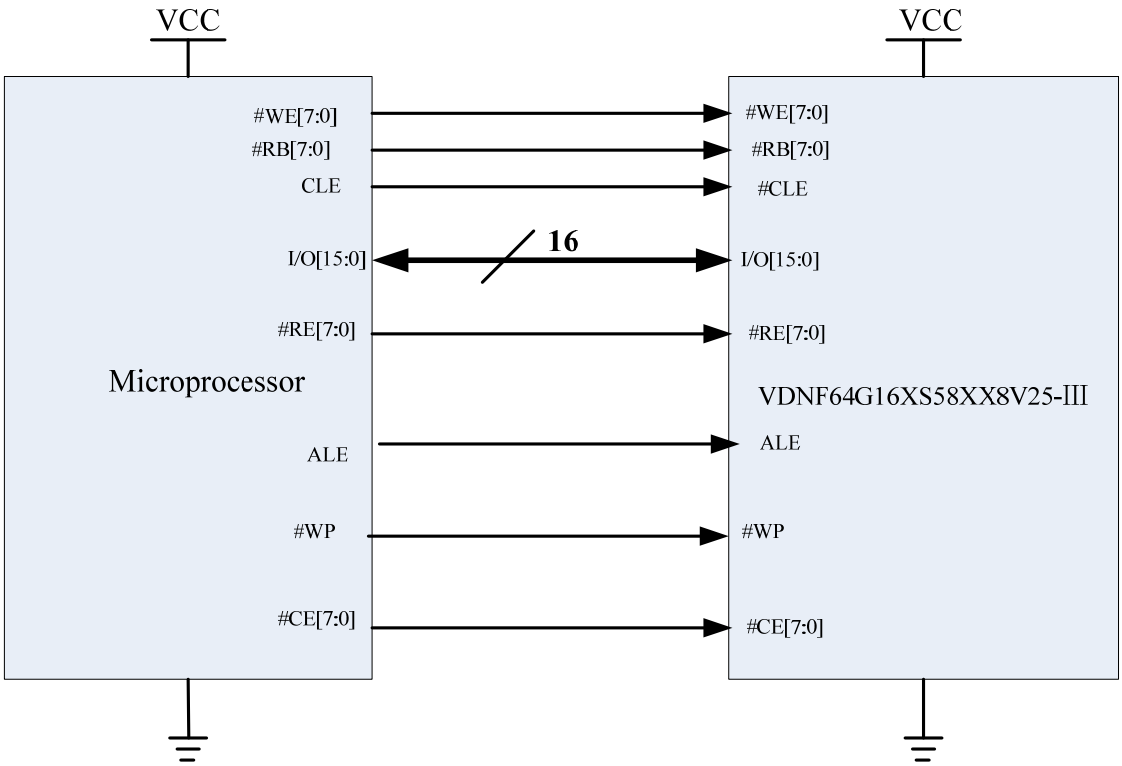

Figure 3 Typical application

7. ORDERING INFORMATION

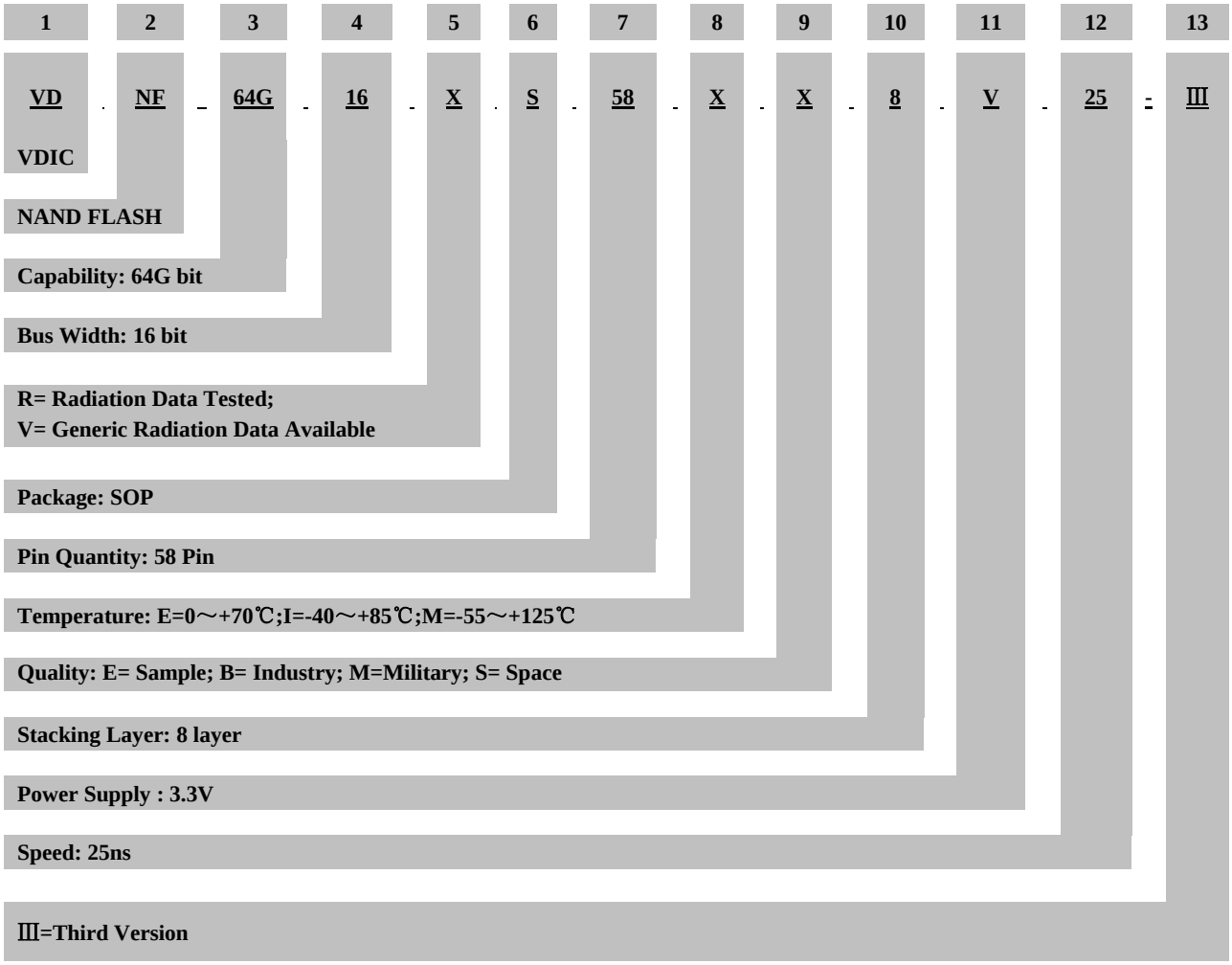

Table 5:Part Information

Part Number	Capacity (bit)	Bus Width (bit)	Radiation			Packaging	Temperature (℃)
			TID[1]	SEL[2]	SEU[3]		
VDNF64G16VS58EE8V25-Ⅲ	64G	16	-	-	-	SOP58	0 ~ + 70
VDNF64G16VS58IB8V25-Ⅲ	64G	16	-	-	-	SOP58	-40 ~ + 85
VDNF64G16VS58MM8V25-Ⅲ	64G	16	-	-	-	SOP58	-55 ~ + 125
VDNF64G16RS58MS8V25-Ⅲ	64G	16	>60	>60	1.3	SOP58	-55 ~ + 125

[1] TID: Total Dose（Krads(Si)）
[2] SEL: LET Threshold（Mev.cm^2/mg）
[3] SEU:SEU Threshold （Mev.cm^2/mg）

8. PACKAGE DIMENSIONS

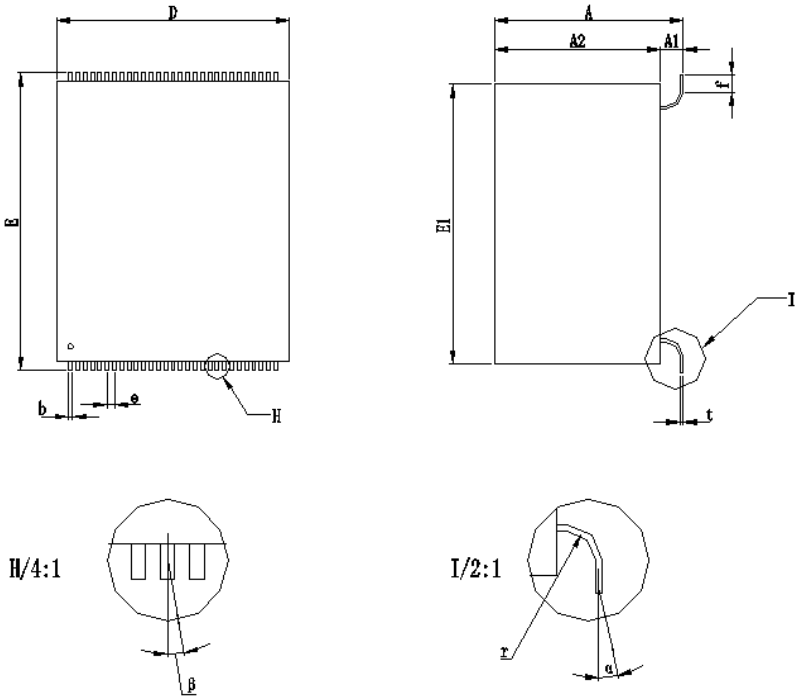

Figure 4 Package dimensions

Table 6 Dimensions information

	Min	Max
A	12.30	12.80
A2	11.10	11.50
D	15.60	16.00
E	19.80	20.20
E1	18.80	19.20
f	1.20	
b	0.25	
e	0.50	
r	1.00	
t	0.20	
α	≤3°	
β	≤3°	
NOTE: 1. Unit: mm 2. A1= A - A2		

9. REVISION HISTORY

Table 7 Revision history

Revision	Date	Description of Change
A0	Sep 29,2018	First Created
A1	Apr 23,2019	Change Block Diagram
A2	Mar 21,2020	Update TID and SEE