VDIC
NAND FLASH MEMORY

VDNF16G08XS50XX2V25
USER MANUAL

Version : A1

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VDIC-NAND Flash Memory

HIGH-SPEED 3.3V 2G×8bit

1. DESCRIPTION

Offered in 2Gx8bit, the VDNF16G08XS50XX2V25 is a 16G-bit NAND Flash Memory with spare capacity of 2048M-byte. The device operates at 3.3V. The I/O pins serve as the ports for address and data input/output as well as command input.

The VDNF16G08XS50XX2V25 device is stacked with two dies. The I/O ports and the control pins(ALE,CLE,#WE,#RE) of each die are connected.

A program operation can be performed in typical 200μs on the (4K+128)Byte page and an erase operation can be performed in typical 1.5ms on a (256K+8K)Byte block. Data in the data register can be read out at 25ns cycle time per Byte.

Every die has an on-chip write controller which is used to automate all program and erase functions including pulse repetition, where required, and internal verification and margining of data. Even the write-intensive systems can take advantage of the VDNF16G08XS50XX2V25′s extended reliability of 100K program/erase cycles by providing ECC(Error Correcting Code) with real time mapping-out algorithm.

Its NAND cell provides the most cost-effective solution for the solid state application market. The VDNF16G08XS50XX2V25 is an optimum solution for large nonvolatile storage applications such as solid state data storage and advanced embedded control applications.

2. FEATURES

- Voltage Supply
    - 3.3V device: 2.7 ~ 3.6 V
- Organization
    - Memory Cell Array
        - 2dies x (1G + 32M)Bytex 8 bit
    - Data Register for each die
        - (4K + 128)Byte x 8bit
- Automatic Program and Erase
    - Page Program for each die
        - (4K + 128)Byte
    - Block Erase for each die
        - (256K + 8K)Byte
- Page Read Operation for each die
    - Page Size

  - (4K + 128)Byte
- Random Access : 25μs(Max.)
- Serial Page Access : 25ns(Min.)

- Fast Write Cycle Time
  - Program time : 200μs(Typ.)
  - Block Erase Time : 1.5ms(Typ.)
- Command/Address/Data Multiplexed I/O Port
- Hardware Data Protection
  - Program/Erase Lockout During Power Transitions
- Reliable CMOS Floating-Gate Technology
  - Endurance : 100K Program/Erase Cycles
  - Data Retention : 10 Years
- Command Register Operation
- Intelligent Copy-Back Opration
- Package TSOP-50

3. BLOCK DIAGRAM

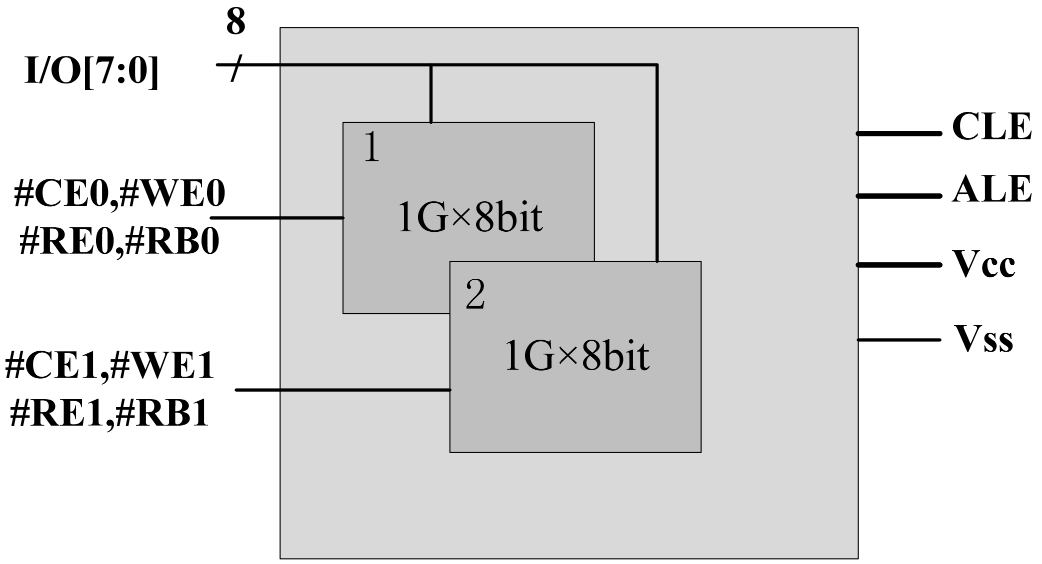

Figure 1 Block diagram

4. PIN DESCRIPTIONS– SOP-50

Pin Id	Pin #			Pin Id
NC	1		50	**NC**
NC	2		49	**NC**
NC	3		48	**NC**
NC	4		47	**NC**
NC	5		46	**NC**
NC	6		45	**I/O7**
#RB1	7		44	**I/O6**
#RB0	8		43	**I/O5**
#RE0	9		42	**I/O4**
#CE0	10		41	**NC**
#CE1	11		40	**#RE1**
NC	12		39	**VCC**
VCC	13		38	**VCC**
VSS	14		37	**VSS**
NC	15		36	**VSS**
NC	16		35	**VSS**
CLE	17		34	**NC**
ALE	18		33	**I/O3**
#WE0	19		32	**I/O2**
#WP	20		31	**I/O1**
#WE1	21		30	**I/O0**
NC	22		29	**NC**
NC	23		28	**NC**
NC	24		27	**NC**
NC	25		26	**NC**

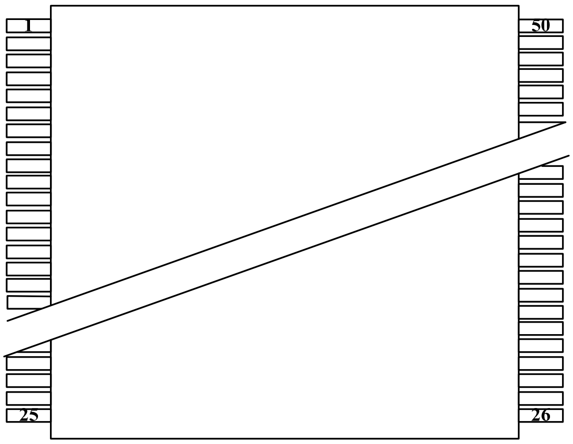

Figure 2 Pin configuration

Table 1: Pin description

Name	Function
I/O0~I/O7	**DATA INPUTS/OUTPUTS** The I/O pins are used to input command, address and data, and to output data during read operations. The I/O pins float to high-z when the chip is deselected or when the outputs are disabled.
CLE	**COMMAND LATCH ENABLE** The CLE input controls the activating path for commands sent to the command register. When active high, commands are latched into the command register through the I/O ports on the rising edge of the #WE signal.
#CE0 (Chip1)	**Chip Enable Input .**When #CEn is Low, the command input cycle becomes valid in chip n. When #CEn is High, all inputs are ignored in chip n.
#CE1 (Chip2)	
ALE	**ADDRESS LATCH ENABLE** The ALE input controls the activating path for the address to the internal address registers. Addresses are latched on the rising edge of #WE with ALE high.
#REn	**READ ENABLE** The #REn input is the serial data-out control, and when active，drives the data onto the I/O bus. Data is valid t_{REA} after the falling edge of #RE which also increments the internal column address counter by one.
#WEn	**WRITE ENABLE** The #WEn input controls writes to the I/O port. Commands, address and data are latched on the rising edge of the #WE pulse.
#WP	**WRITE PROTECT** The #WP pin provides inadvertent write/erase protection during power transitions. The internal high voltage generator is reset when the #WP pin is active low.
#R/B0 (Chip1)	**READY/BUSY OUTPUT** The #R/Bn output indicates the status of the device operation. When low it indicates that a program, erase or random read operation is in process and returns to high state upon completion. It is an open drain output and does not float to high-z condition when the chip is deselected or when outputs are disabled.
#R/B1 (Chip2)	

Name	Function
VCC	**POWER** VCC is the power supply for device.
VSS	**GROUND**

5. ELECTRICAL SPECIFICATIONS

5.1. Absolute Maximum Ratings

Table 2:Absolute Maximum Ratings

Characteristics	Symbol	Maximum ratings	Unit
Voltage on V_{CC} supply relative to Vss	V_{CC}	-0.6 ~ +4.6	V
Voltage on any pin relative to Vss	V_{IN}	-0.6 ~ +4.6	V
Power Dissipation	P_D	1	W
Operating Temperature Range	T_A	-55 ~ +125	℃
Storage Temperature Range	T_{STG}	-65 ~ +150	℃

5.2. Recommended DC Operating Conditions

Table 3:Recommended DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	2.7	3.3	3.6	V
Input high voltage	V_{IH}	$V_{CC}\times0.8$	——	$V_{CC}+0.3$	V
Input low voltage	V_{IL}	-0.3	——	$V_{CC}\times0.2$	V

5.3. DC And Operating Characteristics

Table 4:DC And Operating Characteristics

Parameter	Symbol	Test Conditions	Min	Max	Unit
Output voltage low level	V_{OL}	V_{CC}=2.7V I_{OL} =2.1mA	——	0.4	V
Output voltage high level	V_{OH}	V_{CC}=2.7V,I_{OH}= -0.4mA	2.4	——	V

6. Typical Application

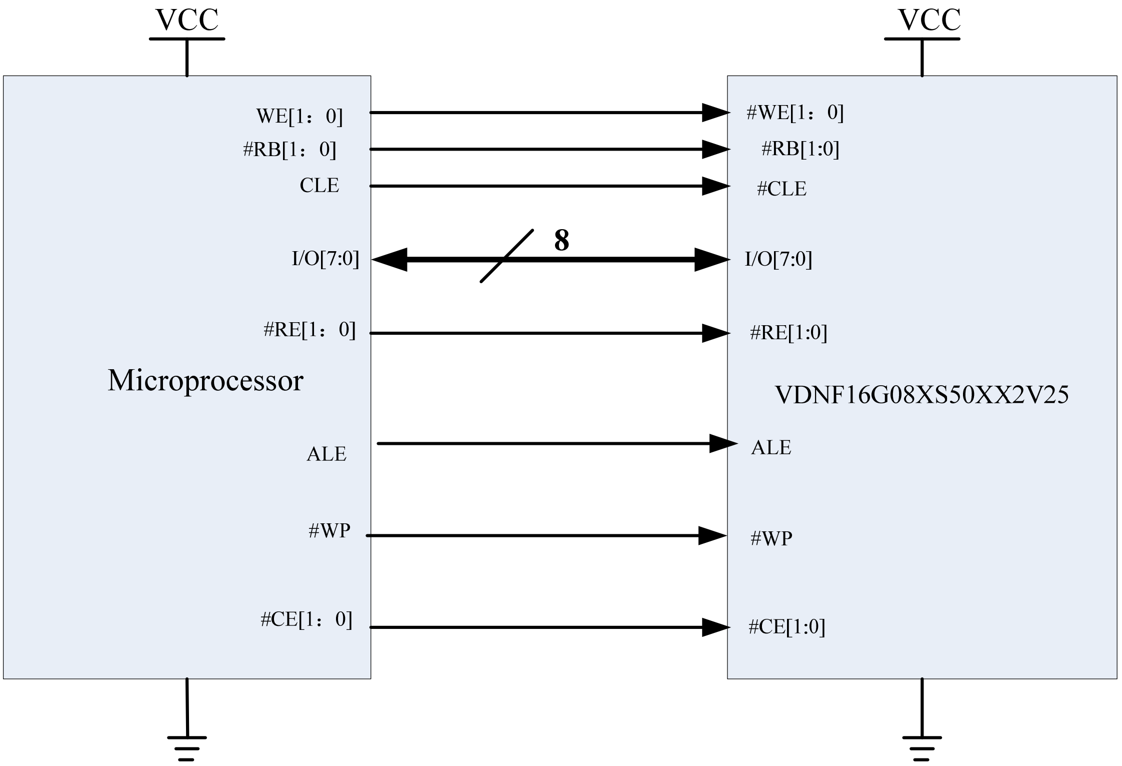

Figure 3 Typical application

7. ORDERING INFORMATION

1	2	3	4	5	6	7	8	9	10	11	12	13
VD	**NF**	**16G**	**08**	**X**	**S**	**50**	**X**	**X**	**2**	**V**	**25**	**_**

VDIC

NAND FLASH

Capability: 16G bit

Bus Width: 8 bit

R= Radiation Data Tested;
V= Generic Radiation Data Available

Package: SOP

Pin Quantity: 50 Pin

Temperature: E=0～+70℃;I=-40～+85℃;M=-55～+125℃

Quality: E= Sample; B= Industry; M=Military; S= Space

Stacking Layer: 2layer

Power Supply : 3.3V

Speed: 25ns

Version: First Version

Table 5:Part Information

Part Number	Capacity (bit)	Bus Width (bit)	Radiation			Packaging	Temperature (℃)
			TID[1]	SEL[2]	SEU[3]		
VDNF16G08VS50EE2V25	16G	8	-	-	-	SOP50	0 ~ + 70
VDNF16G08VS50IB2V25	16G	8	-	-	-	SOP50	-40 ~ + 85
VDNF16G08VS50MM2V25	16G	8	-	-	-	SOP50	-55 ~ + 125
VDNF16G08RS50MS2V25	16G	8	>60	>60	1.3	SOP50	-55 ~ + 125

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[1] TID: Total Dose（Krads(Si)）

[2] SEL: LET Threshold（Mev.cm2/mg）

[3] SEU:SEU Threshold （Mev.cm2/mg）

8. PACKAGE DIMENSIONS

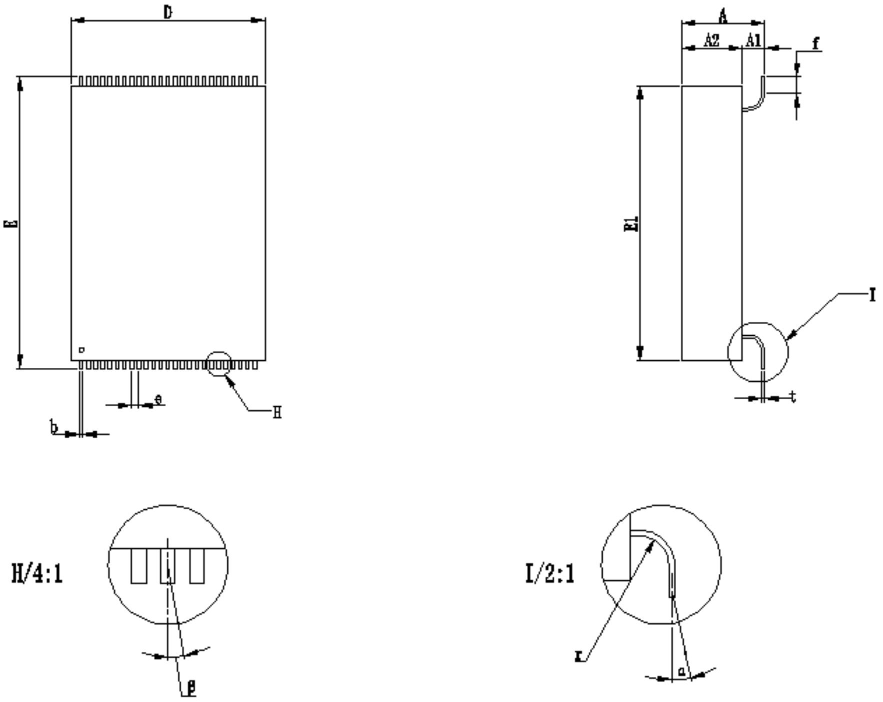

Figure 4 Package dimensions

Table 6 Dimensions information

	Min	**Max**
A	5.20	5.70
A2	4.00	4.40
D	13.30	13.70
E	19.80	20.20
E1	18.80	19.20
f	1.20	
b	0.25	
e	0.50	
r	1.00	
t	0.20	
α	≤3°	
β	≤3°	

NOTE: 1. Unit: mm
2. A1= A - A2

9. REVISION HISTORY

Table 7 Revision history

Revision	Date	Description of Change
A0	Sep 4,2013	First Created
A1	Mar 20,2020	Update TID and SEE