VDIC
NAND FLASH MEMORY

VDNF8G08XS50XX1V25
USER MANUAL

Version A2

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VDIC-NAND Flash Memory

HIGH-SPEED 3.3V 1G × 8bit

1 Description

The VDNF8G08XS50XX1V25 is a 8G-bit NAND Flash Memory device and operates Voltage at 3.3V.

This device contains 1 dies, and the die is offered in 1Gx8bit format and can be operated independently and simultaneously by software. The I/O ports and the control pins (ALE,CLE,#WE,#RE) of the die leading out independently.

This VDNF8G08XS50XX1V25 device include an asynchronous data interface for high-performance I/O operations. These devices use a highly multiplexed 8-bit bus (I/Ox) to transfer commands, address, and data. There are five control signals used to implement the asynchronous data interface: #CE, CLE, ALE, #WE, and #RE. Additional signals control hardware write protection (#WP) and monitor device status (#R/B).

This hardware interface creates a low pin-count device with a standard pin out that remains the same from one density to another, enabling future upgrades to higher densities with no board redesign

The VDNF8G08XS50XX1V25 provides the most cost-effective solution for the solid state application market and is an optimum solution for large nonvolatile storage applications such as solid state data storage and advanced embedded control applications.

2 Features

•Voltage Supply

- 3.3V device: 2.7 ~ 3.6 V

• Organization

- Page size x8 :4320 bytes(4096+224 bytes)
- Block size:128 pages (512K + 25K bytes)
- Plane size:2 planes x1024 blocks per plane
- Device size:8Gb:2048 blocks + 64

• Asynchronous I/O performance

-Up to asynchronous timing mode 4

-tRC/tWC: 25ns (MIN)

• Array performance

- Read page: 25μs (MAX)
- Program page: 230μs (TYP)
- Erase block: 700μs (TYP)

• Operating Voltage Range

- VCC: 2.7–3.6V

- VCCQ: 2.7–3.6V

• Command set: ONFI NAND Flash Protocol

• Advanced Command Set

- Program cache
- Read cache sequential
- Read cache random
- One-time programmable (OTP) mode
- Multi-plane commands
- Multi-LUN operations
- Read unique ID
- Copyback

• First block (block address 00h) is valid when shipped from factory. For minimum required ECC, see Error Management.

• RESET (FFh) required as first command after power- on

• Operation status byte provides software method for detecting

- Operation completion
- Pass/fail condition
- Write-protect status

• Copyback operations supported within the plane from which data is read

• Quality and reliability

- Data retention: 10 years
- Endurance: 100,000 PROGRAM/ERASE cycles

• Operating temperature:

- Automotive Industrial (AIT): –40ºC to +85ºC

• Package

SOP-50

3 Block Diagram

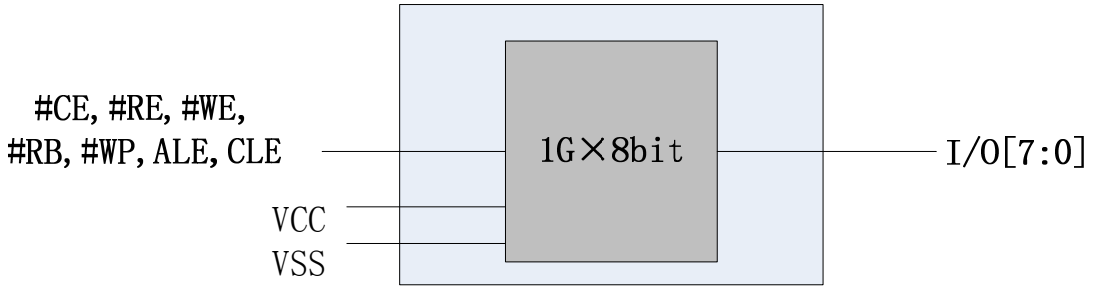

Figure 1 Block diagram

4 Pin Descriptions-sop-50

Pin Id	Pin #		Pin Id
NC	1	50	**NC**
NC	2	49	**NC**
NC	3	48	**NC**
NC	4	47	**NC**
NC	5	46	**NC**
NC	6	45	**I/O7**
NC	7	44	**I/O6**
#RB	8	43	**I/O5**
#RE	9	42	**I/O4**
#CE	10	41	**NC**
NC	11	40	**NC**
NC	12	39	**VCC**
VCC	13	38	**VCC**
VSS	14	37	**VSS**
NC	15	36	**VSS**
NC	16	35	**VSS**
CLE	17	34	**NC**
ALE	18	33	**I/O3**
#WE	19	32	**I/O2**
#WP	20	31	**I/O1**
NC	21	30	**I/O0**
NC	22	29	**NC**
NC	23	28	**NC**
NC	24	27	**NC**
NC	25	26	**NC**

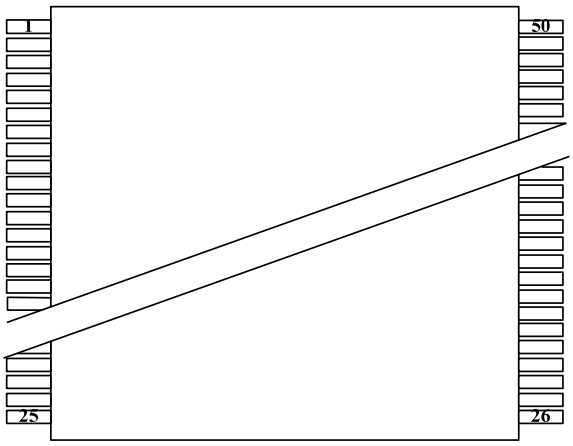

Figure 2 Pin configuration

Table 1: Pin description

Name	Function
I/O0~ I/O7	**DATA INPUTS/OUTPUTS** The I/O pins are used to input command, address and data, and to output data during read operations. The I/O pins float to high-z when the chip is deselected or when the outputs are disabled.
CLE	**COMMAND LATCH ENABLE** The CLE input controls the activating path for commands sent to the command register. When active high, commands are latched into the command register through the I/O ports on the rising edge of the #WE signal.
#CE	**CHIP ENABLE.** When #CE is Low, the command input cycle becomes valid. When #CE is High, all inputs are ignored.
ALE	**ADDRESS LATCH ENABLE** The ALE input controls the activating path for address to the internal address registers. Addresses are latched on the rising edge of #WE with ALE high.
#RE	**READ ENABLE** The #RE input is the serial data-out control, and when active drives the data onto the I/O bus. Data is valid t_{REA} after the falling edge of #RE which also increments the internal column address counter by one.
#WE	**WRITE ENABLE** The #WE input controls writes to the I/O port. Commands, address and data are latched on the rising edge of the #WE pulse.
#WP	**WRITE PROTECT** The #WP pin provides inadvertent write/erase protection during power transitions. The internal high voltage generator is reset when the #WP pin is active low.
#R/B	**READY/BUSY OUTPUT** The #R/B output indicates the status of the device operation. When low, it indicates that a program,

Name	Function
	erase or random read operation is in progress and returns to high state upon completion. It is an open drain output and does not float to high-z condition when the chip is deselected or when outputs are disabled.
VCC	**POWER.**
VSS	**GROUND**

5 Electrical Specifications

Stresses greater than those listed can cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not guar-anteed. Exposure to absolute maximum rating conditions for extended periods can affect reliability

5.1 Absolute Maximum Ratings

Table 2:Absolute Maximum Ratings

Characteristics	Symbol	Maximum ratings	Unit
Supply Voltage relative to V_{SS}	V_{CC}	-0.6 to +4.6	V
Voltage on any Pin relative to V_{SS}	V_{IN}	-0.6 to+4.6	V
Operating Temperature Range	T_{OPR}	-55 to +125	℃
Storage Temperature Range	T_{STG}	-65 to +150	℃

5.2 Recommended DC Operating Conditions

Table 3:Recommended DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
V_{CC} Supply voltage	V_{CC}	2.7	3.3	3.6	V
Input high voltage	V_{IH}	0.8×V_{CC}	——	V_{CC}+0.3	V
Input low voltage	V_{IL}	-0.3	——	0.3×V_{CC}	V

5.3 DC Characteristics and Operating Conditions

Table 4:DC And Operating Characteristics

Parameter	Symbol	Test Conditions	Min	Max	Unit
Low Level Output Voltage	VOL	Vcc=2.7V，I_{OL}=2.1 mA	-	0.4	V
High Level Output Voltage	VOH	Vcc=2.7V，I_{OH}=-0.4mA	2.4	-	V

6 TYPICAL APPLICATION

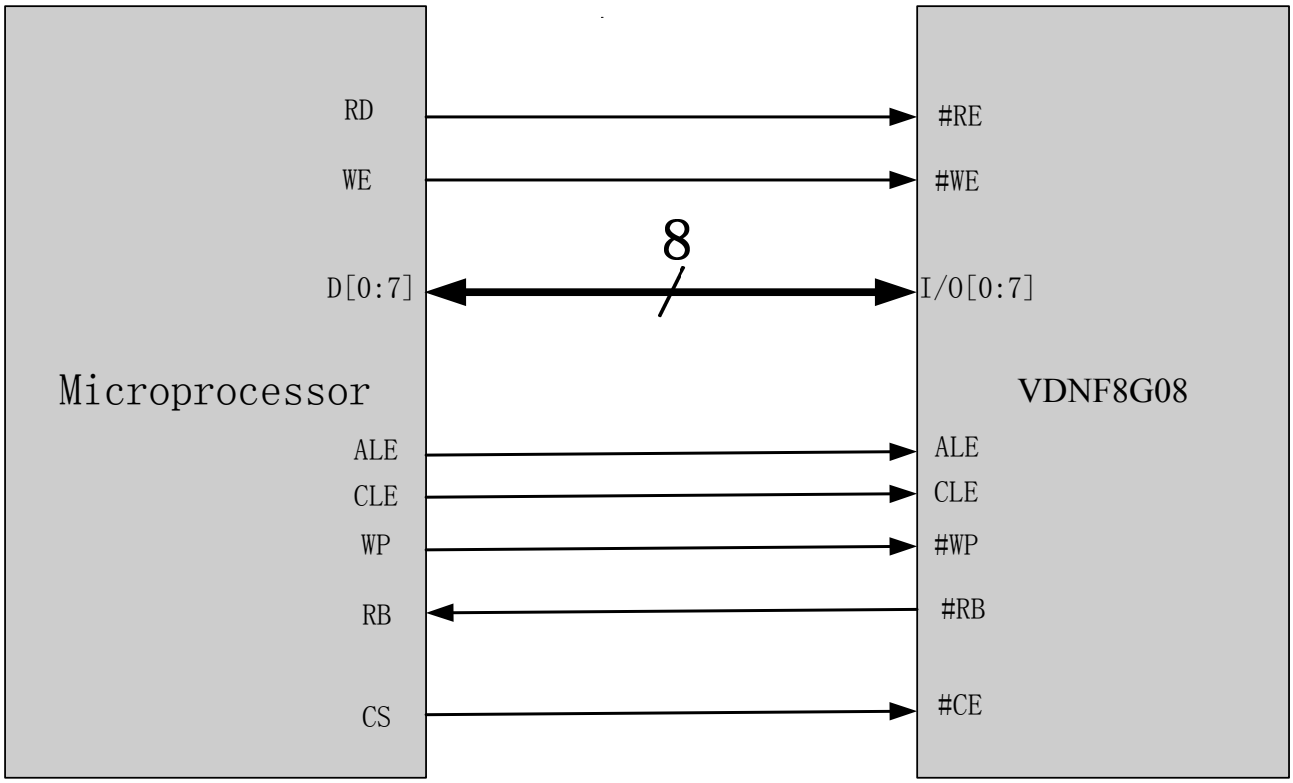

Figure 3 Typical application

7 ORDERING INFORMATION

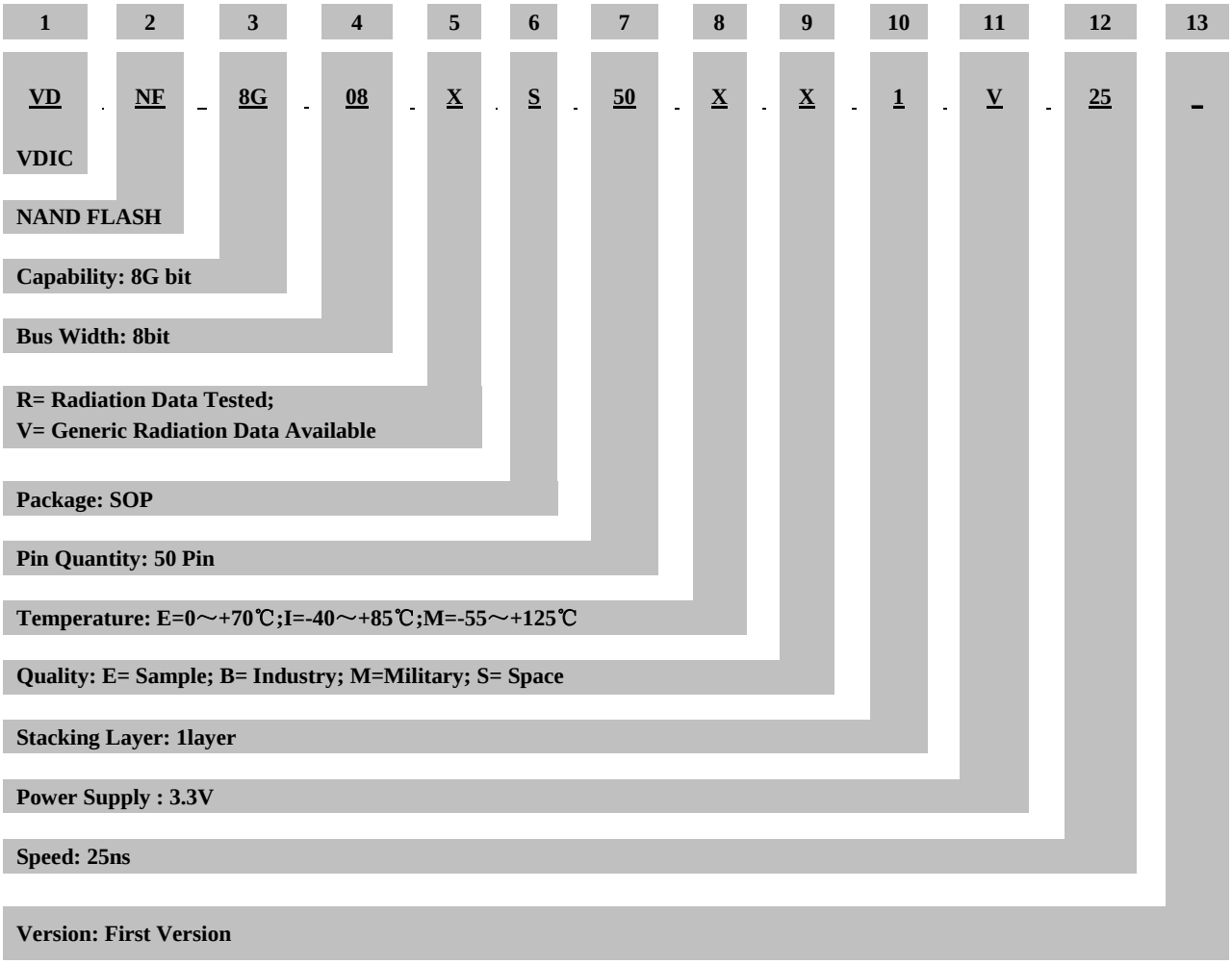

Table 5:Part Information

Part Number	Capacity (bit)	Bus Width (bit)	Radiation			Packaging	Temperature (℃)
			TID[1]	SEL[2]	SEU[3]		
VDNF8G08VS50EE1V25	8G	8	-	-	-	SOP50	0 ~ + 70
VDNF8G08VS50IB1V25	8G	8	-	-	-	SOP50	-40 ~ + 85
VDNF8G08VS50MM1V25	8G	8	-	-	-	SOP50	-55 ~ + 125
VDNF8G08RS50MS1V25	8G	8	>60	>60	1.3	SOP50	-55 ~ + 125

[1] TID: Total Dose（Krads(Si)）
[2] SEL: LET Threshold（Mev.cm2/mg）
[3] SEU:SEU Threshold （Mev.cm2/mg）

8 PACKAGE DIMENSIONS

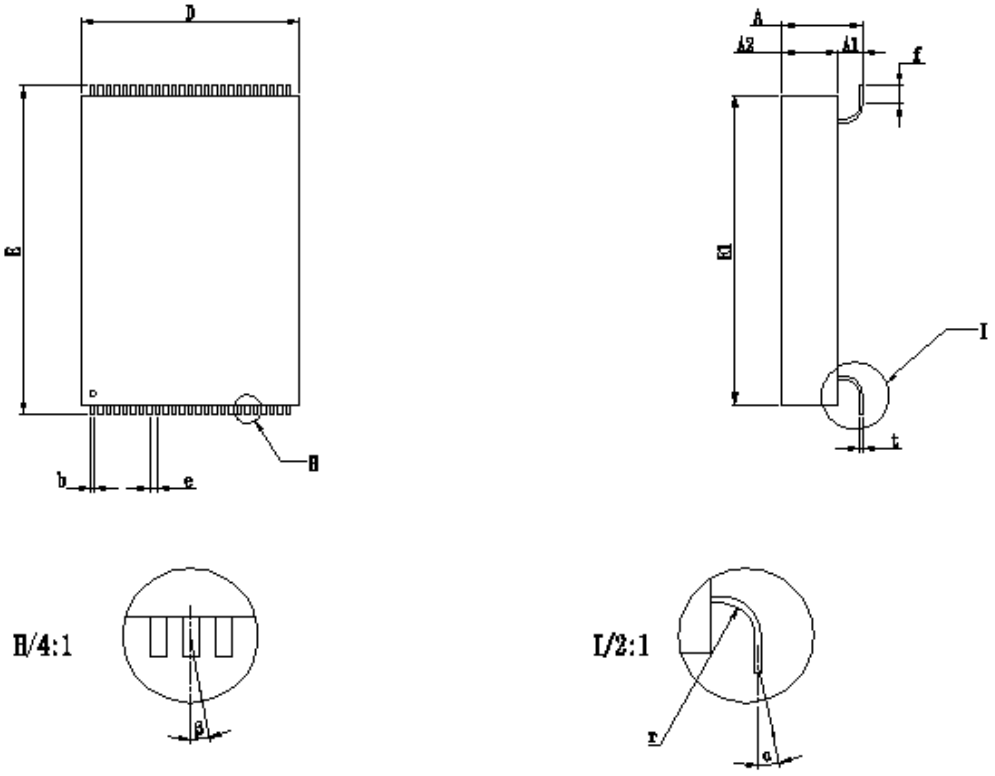

Figure 4 Package dimensions

Table 6 Dimensions information

	Min	Max
A	4.30	5.00
A2	3.10	3.70
D	13.30	13.70
E	19.80	20.20
E1	18.80	19.20
f	1.20	
b	0.25	
e	0.50	
r	1.00	
t	0.20	
α	≤3°	
β	≤3°	
NOTE: 1. Unit: mm 2. A1= A – A2		

9 REVISION HISTORY

Table 7 Revision history

Revision	Date	Description of Change
A0	Feb 1,2018	First Created
A1	May 29,2019	Change Pin Discription
A2	Mar 19,2020	Update TID and SEE