VDIC
NAND Flash Memory

VDNF2T32XP193XX4V25
USER MANUAL

Version : A3

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VDIC-NAND Flash Memory

HIGH-SPEED Asynchronous/Synchronous NAND FALSH 2Tbit

1. DESCRIPTION

The VNDF2T32XP193XX4V25 is a NAND FALSH high-density System-in-Package memory module with a capacity of 2Tb,which is topology of eight packages with a capacity of 256Gb.The memory module transmits commands,address,and data through four groups of multifunctional 8-bit data ports.The control signals(CE#n, CLEn, ALEn, WE#n, and RE#n) used to implement the asynchronous data interface.WP# signal control memory module write protection and (R/B#n) signal monitor package targer status.

This NAND Flash module additionally includes a synchronous data interface for high-performance I/O operations. When the synchronous interface is active, WE#n becomes CLKn and RE#n becomes W/R#n. Data transfers include a bidirectional data strobe (DQSn).

The capacity of each package is 256Gb.Each package consists of four targets,and each target includes two NAND FALSH die(LUN). A NAND Flash die is the minimum unit that can independently execute commands and report status.A target is the unit of memory accessed by a CE#n signal.

The three-dimensional packaging technology is used to interconnect the multi-layer memory circuits to form a high-density NAND FALSH memory module with high reliability ,high stability and miniaturization. It is particularly well suited for use in high reliability,high performance and high density system applications,such as servers or workstations.

2. FEATURES

• Operating Voltage Range

  -V_{CC} : 2.7 ~ 3.6 V

  -V_{CCQ}: 1.7~1.95V

• Open NAND Flash Interface (ONFI) 2.2-compliant

• Single-level cell (SLC) technology

• Organization

  - Memory size 2Tb:8 x packages
  - Package size: 256Gb(32,768 blocks)
  - Block size: 128 pages (1024K + 56K bytes)
  - Page size: 8640 bytes (8192 + 448 bytes)
  - Plane size: 2048 blocks
  - LUN(Die) size: 2 x planes
- Synchronous I/O performance
  - Clock rate: 12ns(DDR)
- Asynchronous I/O performance
  –t RC/ t WC: 25ns(MIN)
- Array performance
  - Read page: 35μs (MAX)
  - Program page: 350μs (TYP)
  - Erase block: 1.5ms (TYP)
- Command set: ONFI NAND Flash Protocol
- RESET (FFh) required as first command after power-on
- Data strobe (DQS) signals provide a hardware meth-od for synchronizing data DQ in the synchronous Interface
- Endurance: 60,000 PROGRAM/ERASE cycles
- Package PGA193
- Available temperature range :

  0℃~+70℃

  -40℃~+85℃

  Specific temperature range can be requested

3. BLOCK DIAGRAM

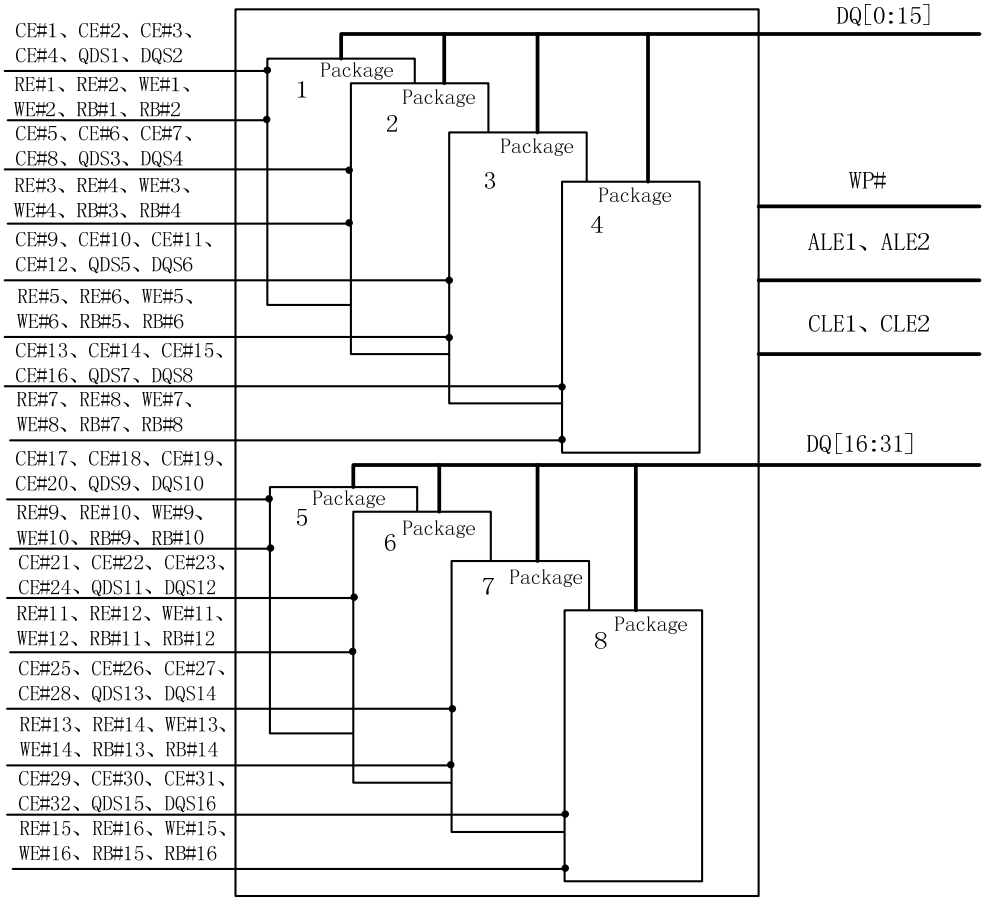


Figure 1:Block Diagram

4. DEVICE ORGANIZATION

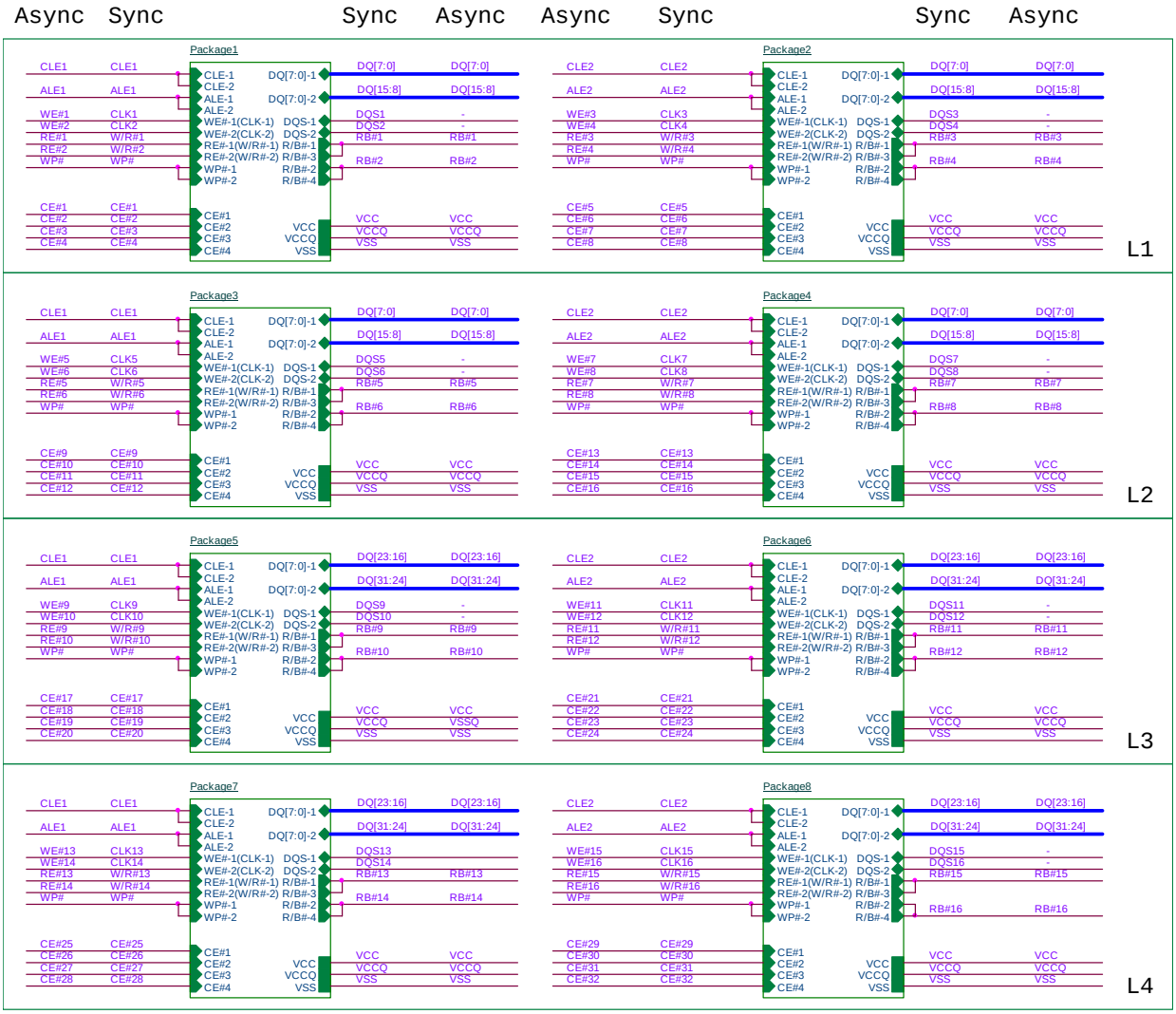


Figure 2:Device Organization

5. PIN DESCRIPTIONS– PGA-193

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A	WP#	CE#3	DQ8	VSS	DQ24	DQ10	DQ18	CE#18	CE#9	RB#2	RB#14	RB#9	DQ21	DQ7	DQ31	CE#7
B	CE#11	CE#19	CE#27	VSS	DQ0	DQ26	CE#2	CE#26	CE#17	RB#6	RB#1	RB#13	DQ13	DQ23	ALE2	CE#15
C	CE#4	CE#12	CE#20	VSS	DQ16	DQ2	CE#10	CE#1	CE#25	RB#10	RB#5	DQ5	DQ29	DQ15	CLE2	CE#23
D	CE#28	ALE1	CLE1	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	CE#31
E	VCC	VCC	VCC	VCC	VSS								VSS	VSS	CE#16	CE#8
F	VCC	VCC	VCC	VCC									VSS	CE#6	CE#32	CE#24
G	VCCQ	VCCQ	VCCQ	VCCQ									VSS	CE#30	CE#22	CE#14
H	DQ25	DQ9	DQ27	VSS									VSS	CE#21	CE#13	CE#5
J	DQ11	DQ17	DQ1	VSS									VSS	RB#8	RB#4	CE#29
K	DQ19	DQ3	DQS14	VSS									VSS	RB#3	RB#16	RB#12
L	DQS10	DQS6	DQS2	VSS									VSS	RB#15	RB#11	RB#7
M	DQS13	DQS9	DQS5	VSS									VSS	VSS	VSS	VSS
N	DQS1	RE#13	RE#9	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS
P	RE#5	RE#6	WE#2	WE#14	WE#9	DQ28	DQ14	DQ22	DQS12	DQS7	WE#4	WE#16	WE#11	RE#16	VSS	VSS
R	RE#1	RE#10	WE#6	WE#1	WE#13	DQ4	DQ30	DQS4	DQS16	DQS11	WE#8	WE#3	WE#15	RE#4	RE#8	RE#12
T	RE#2	RE#14	WE#10	WE#5	DQ12	DQ20	DQ6	DQS8	DQS3	DQS15	WE#12	WE#7	RE#3	RE#7	RE#11	RE#15

TOP VIEW

Figure 3:Signal Assignments

Table 1:Signal Descriptions

Asynchronous signal	Synchronous signal	Type	Function
DQ0~DQ31	DQ0~DQ31	I/O	Data inputs/outputs: The bidirectional I/Os transfer address, data, and command information.
CLE1、CLE2	CLE1、CLE2	Input	Command latch enable: Loads a command from DQn into the command register.
CE#1 ~CE#32	CE#1 ~CE#32	Input	Chip enable: Enables or disables two die in a package's target.
ALE1、ALE2	ALE1、ALE2	Input	Address latch enable: Loads an address from DQn into the address register.
RE#1~RE#16	W/R#1~W/R#16	Input	Read enable and write/read: RE# n transfers serial data from the NAND Flash to the host system when the asynchronous interface is active. When the synchronous interface is active, W/R#n controls the direction of DQn and DQSn.
-	DQS1~DQS16	I/O	Data strobe: Provides a synchronous reference for data input and output.
WE#1~WE#16	CLK1~CLK16	Input	Write enable and clock: WE#n transfers commands, addresses, and serial data from the host system to the NAND Flash when the asynchronous interface is active. When the synchronous interface is active, CLKn latches command and address cycles.

Asynchronous signal	Synchronous signal	Type	Function
WP#	WP#	Input	Write protect: Enables or disables array PROGRAM and ERASE operations.
RB#1~RB#16	RB#1~RB#16	Output	Ready/busy: An open-drain, active-low output that requires an external pull-up resistor. This signal indicates target array activity.
V_{CC}	V_{CC}	Supply	V_{CC}: Core power supply,3.3+0.3/-0.6V
V_{CCQ}	V_{CCQ}	Supply	V_{CCQ}: I/O power supply,1.8+0.15/-0.1V
Vss	Vss	Supply	Vss: Ground connection

6. ELECTRICAL SPECIFICATIONS

6.1. Absolute Maximum Ratings

Table 2:Absolute Maximum Ratings

Characteristics	Symbol	Maximum ratings	Unit
Voltage on V_{CC} supply relative to Vss	V_{CC}	-0.6 to +4.6	V
Voltage on V_{CCQ} supply relative to Vss	V_{CCQ}	-0.6 to +4.6	V
Voltage on any pin relative to Vss	V_{IN}	-0.6 to +4.6	V
Power Dissipation	PD	2.0	W
Storage Temperature Range	TSTG	-65 to +150	℃

Notes:1. Voltage on any pin relative to V SS

6.2. Recommended DC Operating Conditions

Table 3:Recommended DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
V_{CC} Supply voltage	V_{CC}	2.7	3.3	3.6	V
V_{CCQ} supply voltage	V_{CCQ}	1.7	1.8	1.95	V
AC Input high voltage	$V_{IH(AC)}$	0.8xV_{CCQ}	-	V_{CCQ}+0.3	V
DC Input high voltage	$V_{IH(DC)}$	0.7xV_{CCQ}	-	V_{CCQ}+0.3	V
AC Input low voltage	$V_{IL(AC)}$	-0.3	-	0.2xV_{CCQ}	V

Parameter	Symbol	Min	Typ	Max	Unit
DC Input low voltage	$V_{IL(DC)}$	-0.3	-	0.3xV_{CCQ}	V

6.3. DC And Operating Characteristics

Asynchronous Mode

Table 4:DC And Operating Characteristics(Asynchronous Mode)

Parameter	Symbol	Test Conditions	Min	Max	Unit
Output voltage low level	V_{OL}	V_{CC}=3.6V,V_{CCQ}=1.95V,I_{OL} =2.1mA	—	0.3xV_{CCQ}	V
Output voltage high level	V_{OH}	V_{CC}=2.7V,V_{CCQ}=1.7V,I_{OH}= -0.4mA	0.7xV_{CCQ}	—	V

Synchronous Mode

Table 5:AC And Operating Characteristics(Synchronous Mode)

Parameter	Symbol	Test Conditions	Min	Max	Unit
Output voltage low level	V_{OL}	V_{CC}=3.6V,V_{CCQ}=1.95V,I_{OL} =2.1mA	—	0.2xV_{CCQ}	V
Output voltage high level	V_{OH}	V_{CC}=2.7V,V_{CCQ}=1.7V,I_{OH}= -0.4mA	0.8xV_{CCQ}	—	V

7. TYPICAL APPLICATION

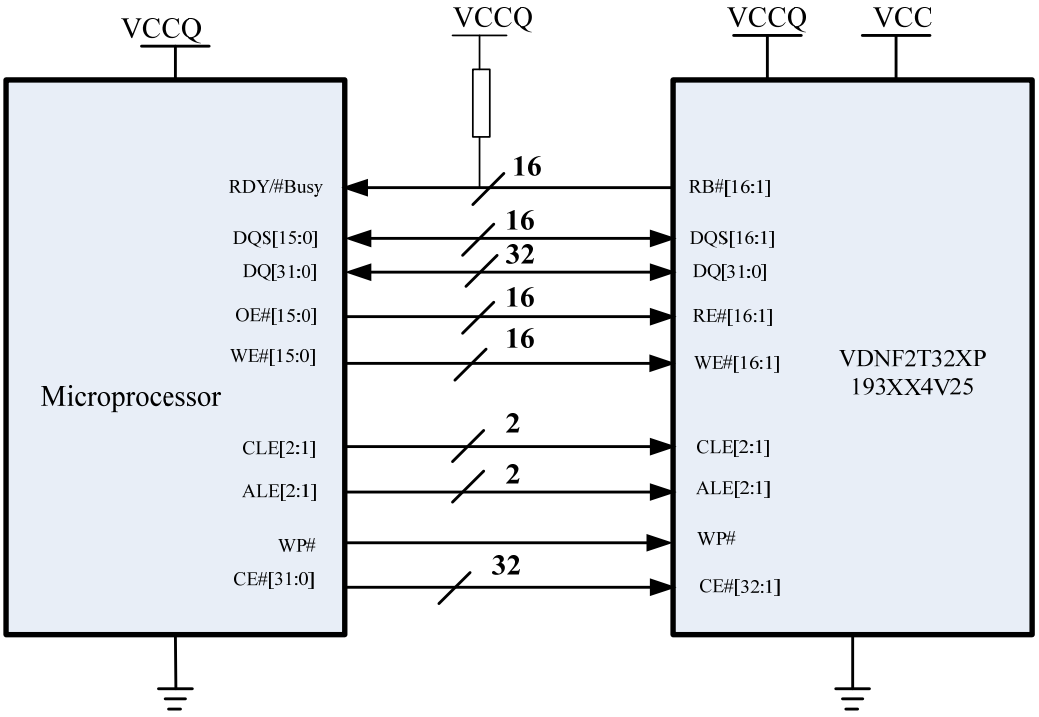


Figure 4:Typical Application

Table 6: Recommended Signal Combination

Group	Signal Combination								
1	CE#1	DQ[7:0]	CLE1	ALE1	DQS1	WE#1	RE#1	RB#1	WP#
	CE#2	DQ[15: 8]			DQS2	WE#2	RE#2	RB#2	
	CE#17	DQ[23:16]			DQS9	WE#9	RE#9	RB#9	
	CE#18	DQ[31:24]			DQS10	WE#10	RE#10	RB#10	
2	CE#3	DQ[7:0]	CLE1	ALE1	DQS1	WE#1	RE#1	RB#1	
	CE#4	DQ[15: 8]			DQS2	WE#2	RE#2	RB#2	
	CE#19	DQ[23:16]			DQS9	WE#9	RE#9	RB#9	
	CE#20	DQ[31:24]			DQS10	WE#10	RE#10	RB#10	
3	CE#5	DQ[7:0]	CLE2	ALE2	DQS3	WE#3	RE#3	RB#3	
	CE#6	DQ[15: 8]			DQS4	WE#4	RE#4	RB#4	
	CE#21	DQ[23:16]			DQS11	WE#11	RE#11	RB#11	
	CE#22	DQ[31:24]			DQS12	WE#12	RE#12	RB#12	
4	CE#7	DQ[7:0]	CLE2	ALE2	DQS3	WE#3	RE#3	RB#3	
	CE#8	DQ[15: 8]			DQS4	WE#4	RE#4	RB#4	
	CE#23	DQ[23:16]			DQS11	WE#11	RE#11	RB#11	
	CE#24	DQ[31:24]			DQS12	WE#12	RE#12	RB#12	
5	CE#9	DQ[7:0]	CLE1	ALE1	DQS5	WE#5	RE#5	RB#5	
	CE#10	DQ[15: 8]			DQS6	WE#6	RE#6	RB#6	
	CE#25	DQ[23:16]			DQS13	WE#13	RE#13	RB#13	
	CE#26	DQ[31:24]			DQS14	WE#14	RE#14	RB#14	
6	CE#11	DQ[7:0]	CLE1	ALE1	DQS5	WE#5	RE#5	RB#5	
	CE#12	DQ[15: 8]			DQS6	WE#6	RE#6	RB#6	
	CE#27	DQ[23:16]			DQS13	WE#13	RE#13	RB#13	
	CE#28	DQ[31:24]			DQS14	WE#14	RE#14	RB#14	
7	CE#13	DQ[7:0]	CLE2	ALE2	DQS7	WE#7	RE#7	RB#7	
	CE#14	DQ[15: 8]			DQS8	WE#8	RE#8	RB#8	
	CE#29	DQ[23:16]			DQS15	WE#15	RE#15	RB#15	
	CE#30	DQ[31:24]			DQS16	WE#16	RE#16	RB#16	
8	CE#15	DQ[7:0]	CLE2	ALE2	DQS7	WE#7	RE#7	RB#7	
	CE#16	DQ[15: 8]			DQS8	WE#8	RE#8	RB#8	
	CE#31	DQ[23:16]			DQS15	WE#15	RE#15	RB#15	
	CE#32	DQ[31:24]			DQS16	WE#16	RE#16	RB#16	

8. ORDERING INFORMATION

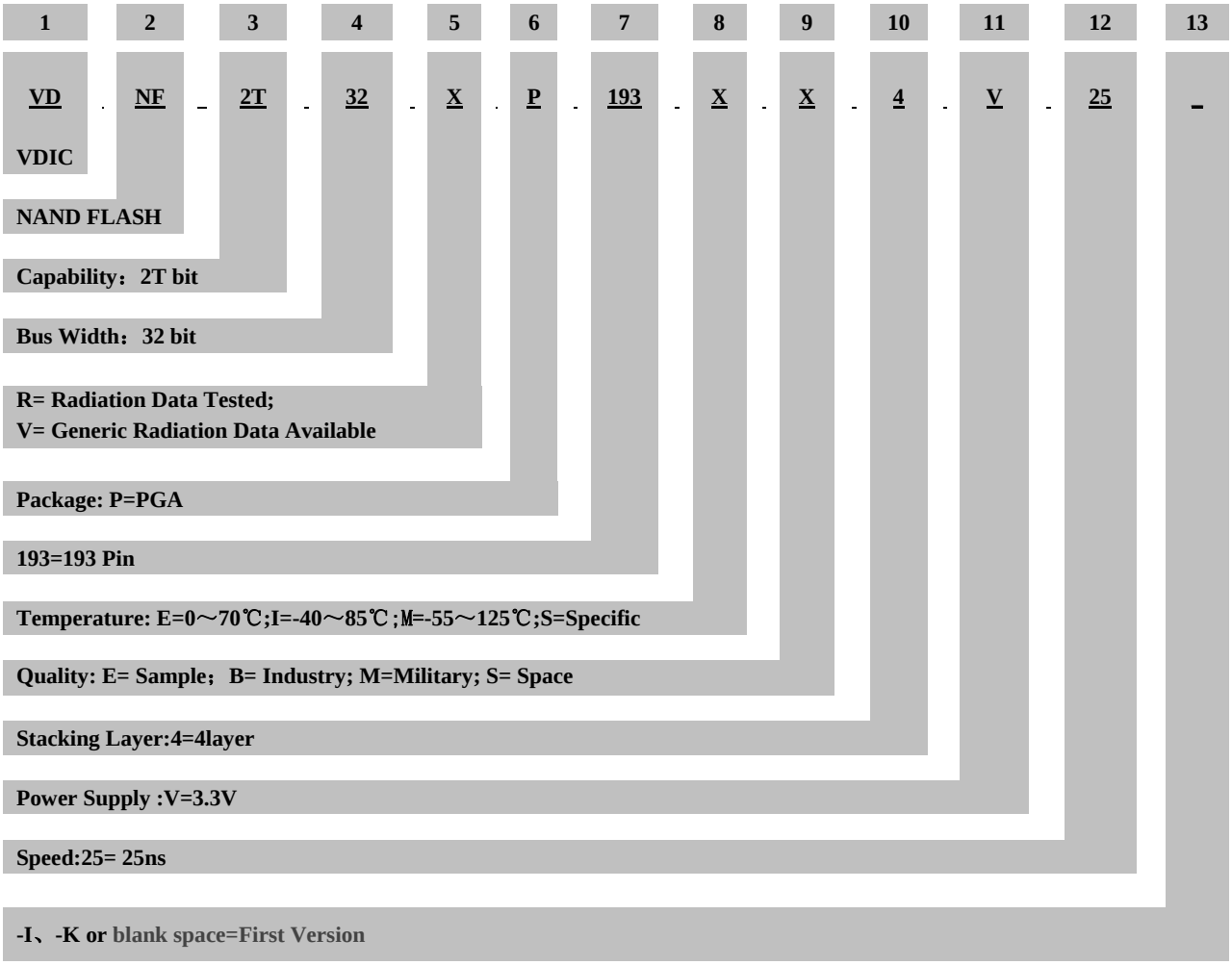
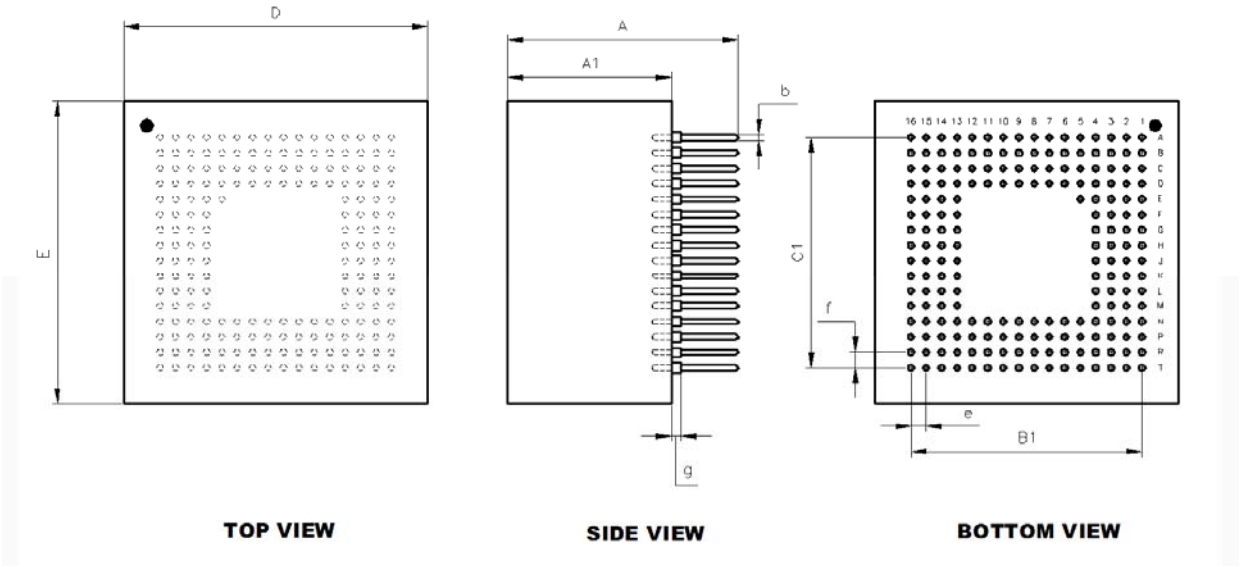


Table 6:Part Information

Part Number	Capacity (bit)	Bus Width (bit)	Radiation			Packaging	Temperature (℃)
			TID[1]	SEL[2]	SEU[3]		
VDNF2T32VP193EE4V25	2T	32	-	-	-	PGA193	0 ~ + 70
VDNF2T32VP193IB4V25	2T	32	-	-	-	PGA193	-40 ~ + 85
VDNF2T32RP193SS4V25	2T	32	TBD	TBD	TBD	PGA193	-55 ~ + 105

[1] TID: Total Dose（Krads(Si)）
[2] SEL: LET Threshold（Mev.cm2/mg）
[3] SEU:SEU Threshold （Mev.cm2/mg）

9. DEVICE DIMENSIONS



	Min	Max
A	18.7	19.3
A1	13.2	13.8
D	25.8	26.2
E	25.8	26.2
B1	e*15	
C1	f*15	
b	0.46±0.05	
e	1.27	
f	1.27	
g	0.8	
NOTE：1. Unit：mm		

Figure 5:Device Dimensions

10. REVISION HISTORY

Revision	Date	Description of Change
A0	Jun 3,2017	First Created
A1	Mar 27,2018	Add or reduce chapters
A2	May 22,2018	Modified FEATURES
A3	Mar.,2020	Fix some content