VDIC
NAND FLASH MEMORY

VDNF2G08XS48XX1V25
USER MANUAL

Version : B0

Document NO.： ORBITA/SIP- VDNF2G08XS48XX1V25-USM-01
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VDIC-NAND Flash Memory

3.3V 256M × 8bit

1. DESCRIPTION

Offered in 256M × 8bit , the VDNF2G08XS48XX1V25 is a 2G bit NAND Flash Memory with spare capacity of 64M-bits. The device operates at 3.3V. The I/O pins serve as the ports for address and data input/output as well as command input.

The VDNF2G08XS48XX1V25 is stacked with one die, the die consisting of 256M × 8bit. a program operation can be performed in typical 200μs on a (2K+64)byte page and an erase operation can be performed in typical 1.5ms on a (128K+4K)byte block. Data in the page can be read out at 25ns cycle time per byte.

The device has an on-chip write controller which is used to automate all program and erase functions including pulse repetition, where required, and internal verification and margining of data. Even the write-intensive systems can take advantage of the VDNF2G08XS48XX1V25′s extended reliability of 100K program/erase cycles by providing ECC(Error Correcting Code) with real time mapping-out algorithm.

The VDNF2G08XS48XX1V25 is an optimum solution for large nonvolatile storage applications such as solid state data storage and advanced embedded control applications.

2. FEATURES

- Voltage Supply
  - 3.3V device: 2.7 ~ 3.6 V
- Organization
  - Memory Cell Array
  - 1die ×(256M + 8M) × 8 bit
  - Data Register
  - (2K + 64) × 8bit
- Automatic Program and Erase
  - Page Program
- -(2K + 64)Byte
  - Block Erase
  - (128K + 4K)Byte
- Page Read Operation
  - Page Size
  - (2K + 64)Byte
  - Random Access : 25μs(Max.)
  - Serial Page Access : 25ns(Min.)
- Fast Write Cycle Time
  - Program time : 200μs(Typ.)
  - Block Erase Time : 1.5ms(Typ.)
- Command/Address/Data Multiplexed I/O Port
- Hardware Data Protection
  - Program/Erase Lockout During Power Transitions
- Reliable CMOS Floating-Gate Technology
  - Endurance : 100K Program/Erase Cycles
  - Data Retention : 10 Years

- Command Register Operation
- Intelligent Copy-Back with internal 1bit/528Byte EDC
- Package: SOP-48

3. Block Diagram

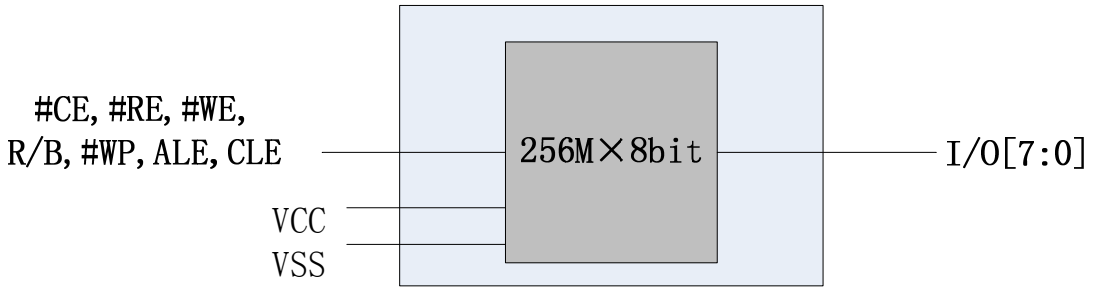

Figure 1 Block diagram

4. PIN DESCRIPTIONS–SOP-48

Pin Id	Pin #		Pin Id
NC	1	48	**NC**
NC	2	47	**NC**
NC	3	46	**NC**
NC	4	45	**NC**
NC	5	44	**I/O7**
NC	6	43	**I/O6**
R/B	7	42	**I/O5**
#RE	8	41	**I/O4**
#CE	9	40	**NC**
NC	10	39	**NC**
NC	11	38	**NC**
VCC	12	37	**VCC**
VSS	13	36	**VSS**
NC	14	35	**NC**
NC	15	34	**NC**
CLE	16	33	**NC**
ALE	17	32	**I/O3**
#WE	18	31	**I/O2**
#WP	19	30	**I/O1**
NC	20	29	**I/O0**
NC	21	28	**NC**
NC	22	27	**NC**
NC	23	26	**NC**
NC	24	25	**NC**

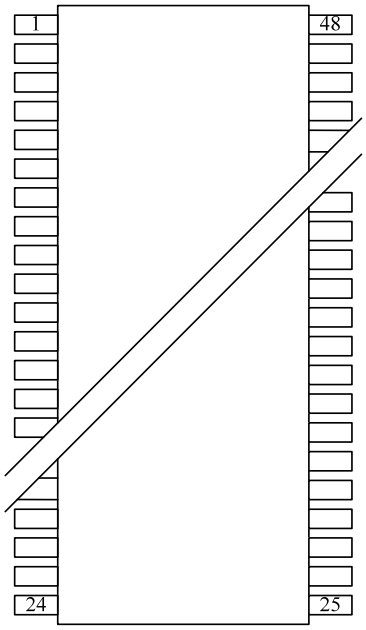

Figure 2 Pin configuration

Table 1: Pin description

Name	Function
I/O0~I/O7	**DATA INPUTS/OUTPUTS** The I/O pins are used to input command, address and data, and to output data during read operations. The I/O pins float to high-z when the chip is deselected or when the outputs are disabled.
CLE	**COMMAND LATCH ENABLE** The CLE input controls the activating path for commands sent to the command register. When active high, commands are latched into the command register through the I/O ports on the rising edge of the #WE signal.
#CE	**Chip Enable Input** When #CE is Low, the command input cycle becomes valid. When #CE is High, all inputs are ignored.
ALE	**ADDRESS LATCH ENABLE** The ALE input controls the activating path for address to the internal address registers. Addresses are latched on the rising edge of #WE with ALE high.
#RE	**READ ENABLE** The #RE input is the serial data-out control, and when active drives the data onto the I/O bus. Data is valid tREA after the falling edge of #RE which also increments the internal column address counter by one.
#WE	**WRITE ENABLE** The #WE input controls writes to the I/O port. Commands, address and data are latched on the rising edge of the #WE pulse.
#WP	**WRITE PROTECT** The #WP pin provides inadvertent write/erase protection during power transitions. The internal high voltage generator is reset when the #WP pin is active low.
R/B	**READY/BUSY OUTPUT** The R/B output indicates the status of the device operation. When low, it indicates that a program, erase or random read operation is in progress and returns to high state upon completion. It is an open drain output and does not float to high-z condition when the chip is deselected or when outputs are disabled.
VCC	**POWER** VCC is the power supply for device.
VSS	GROUND
NC	**NO CONNECTION** Lead is not internally connected.

5. ELECTRICAL SPECIFICATIONS

5.1. Absolute Maximum Ratings

Table 2:Absolute Maximum Ratings

Characteristics	Symbol	Maxinmum ratings	Unit
Voltage on VCC supply relative to Vss	V_{CC}	-0.6 ~ +4.6	V
Voltage on any pin relative to Vss	V_{IN}	-0.6 ~ +4.6	V
	$V_{I/O}$	-0.6 ~ V_{CC} +0.3(< 4.6)	V
Power Dissipation	P_D	0.5	W
Operating Temperature Range	T_{OPR}	-55 ~ +125	℃
Storage Temperature Range	T_{STG}	-65 ~ +150	℃

5.2. Recommended DC Operating Conditions

Table 3:Recommended DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	2.7	3.3	3.6	V
Input high voltage	V_{IH}	V_{CC}×0.8	——	V_{CC}+0.3	V
Input low voltage	V_{IL}	-0.3	——	0.8	V

5.3. DC and Operating Characteristics

Table 4:DC And Operating Characteristics

Parameter	Symbol	Test Conditions	Min	Max	Unit
Output voltage low level	V_{OL}	V_{CC}=2.7V，I_{OL}=+4mA	——	0.4	V
Output voltage high level	V_{OH}	V_{CC}=2.7V，I_{OH}=-2mA	2.4	——	V

6. Typical Application

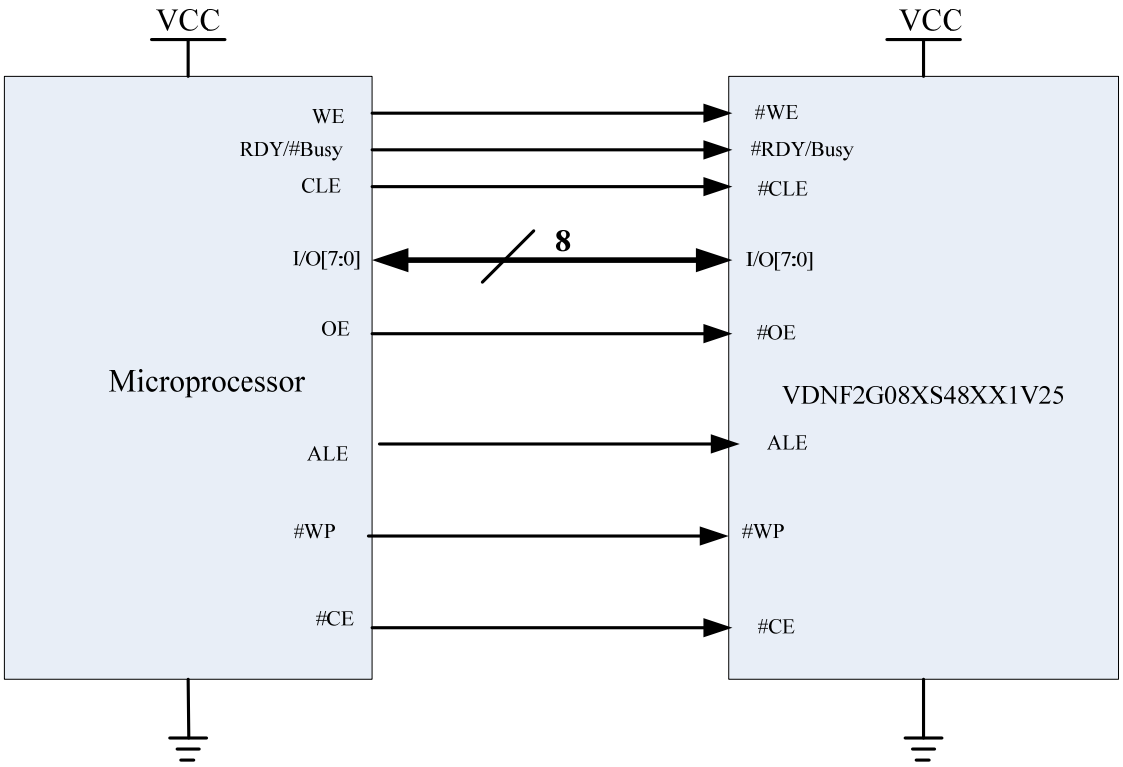

Figure 3 Typical application

7. ORDERING INFORMATION

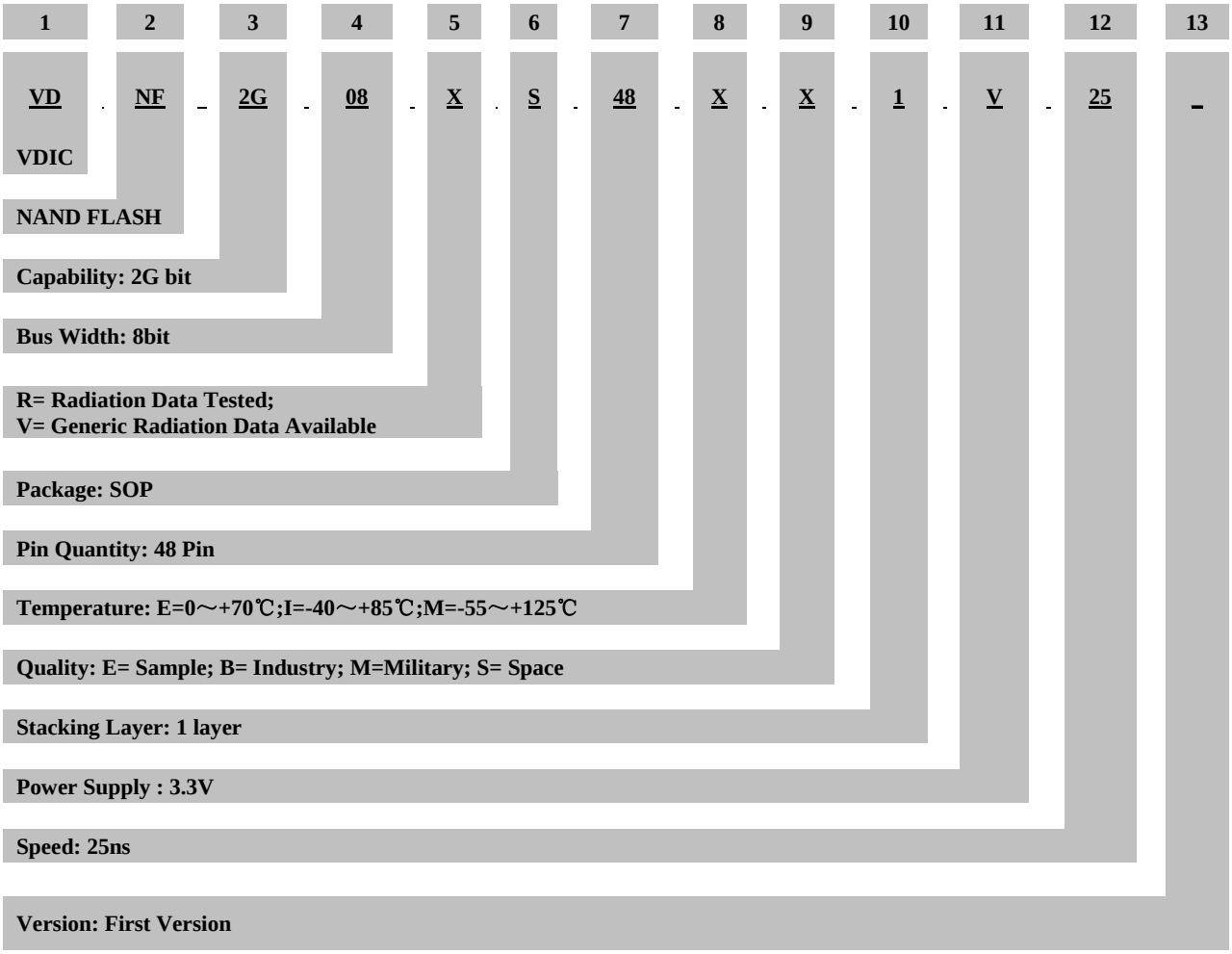

Table 5:Part Information

Part Number	Capacity (bit)	Bus Width (bit)	Radiation			Packaging	Temperature (℃)
			TID[1]	SEL[2]	SEU[3]		
VDNF2G08VS48EE1V25	2G	8	-	-	-	SOP48	0 ~ + 70
VDNF2G08VS48IB1V25	2G	8	-	-	-	SOP48	-40 ~ + 85
VDNF2G08VS48MM1V25	2G	8	-	-	-	SOP48	-55 ~ + 125
VDNF2G08RS48MS1V25	2G	8	TBD	TBD	TBD	SOP48	-55 ~ + 125

[1] TID: Total Dose（Krads(Si)）
[2] SEL: LET Threshold（Mev.cm2/mg）
[3] SEU:SEU Threshold （Mev.cm2/mg）

8. PACKAGE DIMENSIONS

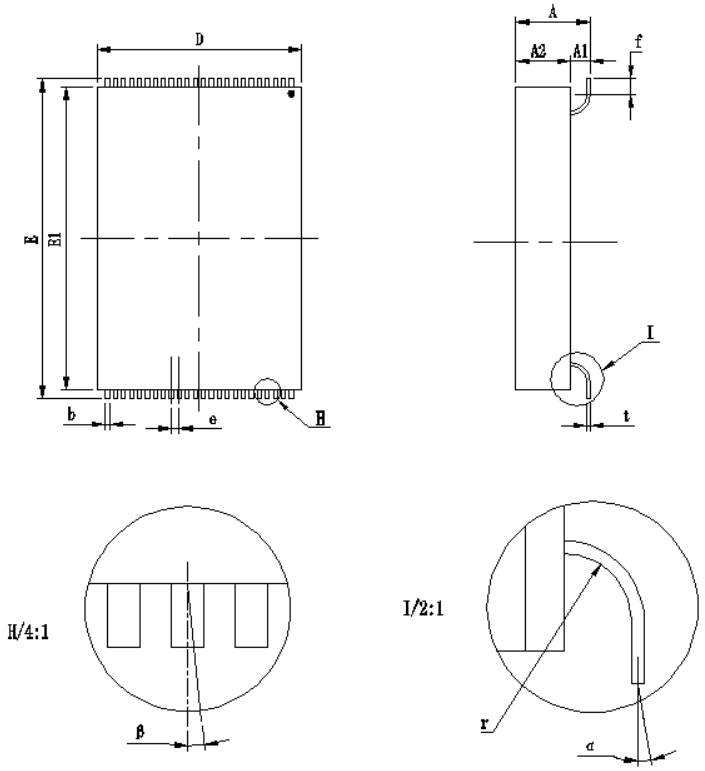

Figure 4 Package dimensions

Table 6 Dimensions information

	Min	Max
A	3.70	4.40
A2	2.50	3.10
D	12.70	13.10
E	19.80	20.20
E1	18.80	19.20
f	1.20	
b	0.25	
e	0.50	
r	1.00	
t	0.20	
α	≤3°	
β	≤3°	
NOTE: 1. Unit: mm 2. A1= A - A2		

9. REVISION HISTORY

Table 7 Revision history

Revision	Date	Description of Change
A0	Nov 3,2015	First Created
A1	Mar 14,2016	Modified the PIN DESCRIPTIONS
A2	Aug 23,2016	Modified the ORDERING INFORMATION
A3	Jan 9,2017	Modified the PACKAGE DIMENSIONS
A4	Oct.25,2017	Changed company's name to Zhuhai Orbita Aerospace Science & Technology Co.，Ltd
A5	Mar 24,2018	Add or reduce chapters
B0	Mar 19,2020	Update TID and SEE