VDIC
NAND FLASH MEMORY

HKNF8G08VS48MM1V25
USER MANUAL

Version : A0

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VDIC-NAND Flash Memory

HIGH-SPEED 3.3V 1G×8bit

1. DESCRIPTION

Offered in 1Gx8bit, the HKNF8G08VS48MM1V25 is a 8G-bit NAND Flash Memory with spare capacity of 448M-bits. The device operates at 3.3V. The I/O pins serve as the ports for address and data input/output as well as command input.

The HKNF8G08VS48MM1V25 device is stacked with one dies. The I/O ports and the control pins (ALE,CLE,#WE,#RE) of each die are connected.

A program operation can be performed in typical 230µs on the (4K+224)Byte page and an erase operation can be performed in typical 0.7ms on a (512K+28K)Byte block. Data in the data register can be read out at 25ns cycle time per Byte.

The device has an on-chip write controller which is used to automate all program and erase functions including pulse repetition, where required, and internal verification and margining of data. Even the write-intensive systems can take advantage of the HKNF8G08VS48MM1V25 's extended reliability of 100K program/erase cycles by providing ECC(Error Correcting Code) with real time mapping-out algorithm.

Its NAND cell provides the most cost-effective solution for the solid state application market. The HKNF8G08VS48MM1V25 is an optimum solution for large nonvolatile storage applications such as solid state data storage and advanced embedded control applications.

2. FEATURES

- Voltage Supply
  - 3.3V device: 2.7 ~ 3.6 V
- Organization
  - Page size x8 :4320 bytes(4096+224 bytes)
  - Block size:128 pages (512K + 25K bytes)
  - Plane size:2 planes x1024 blocks per plane
  - Device size:8Gb:2048 blocks + 64
- Asynchronous I/O performance
  - Up to asynchronous timing mode 4
  - tRC/tWC: 25ns (MIN)
- Array performance
  - Read page: 25µs (MAX)
  - Program page: 230µs (TYP)
  - Erase block: 700µs (TYP)
- Operating Voltage Range
  - VCC: 2.7–3.6V
  - VCCQ: 2.7–3.6V
- Command set: ONFI NAND Flash Protocol
- Advanced Command Set
  - Program cache
  - Read cache sequential
  - Read cache random
  - One-time programmable (OTP) mode
  - Multi-plane commands
  - Multi-LUN operations
  - Read unique ID
  - Copyback
- First block (block address 00h) is valid when shipped from factory. For minimum required ECC, see Error Management (page 86).
- RESET (FFh) required as first command after power- on
- Operation status byte provides software method for detecting
  - Operation completion
  - Pass/fail condition
  - Write-protect status
- Copyback operations supported within the plane from which data is read
- Quality and reliability
  - Data retention: 10 years
  - Endurance: 100,000 PROGRAM/ERASE cycles
- Operating temperature:
  - Automotive Industrial (AIT): –40ºC to +85ºC
- Package
  - 48-pin TSOP

3. Block Diagram

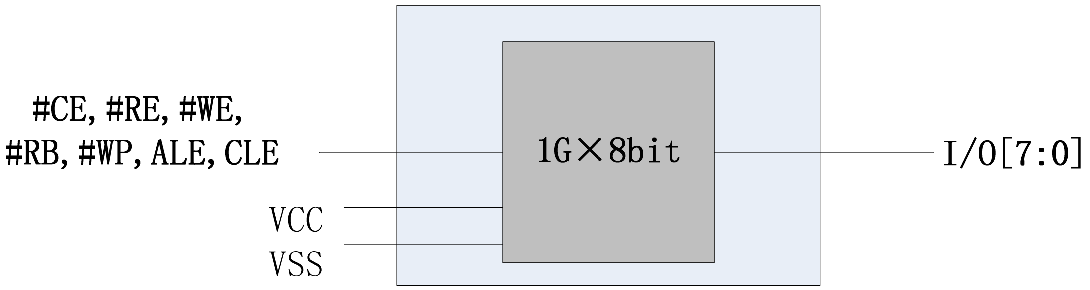

Figure 1:Block Diagram

4. PIN DESCRIPTIONS-sop-48

Pin Id	Pin #			Pin Id
NC	1		48	**NC**
NC	2		47	**NC**
NC	3		46	**NC**
NC	4		45	**NC**
NC	5		44	**I/O7**
NC	6		43	**I/O6**
#R/B	7		42	**I/O5**
#RE	8		41	**I/O4**
#CE	9		40	**NC**
NC	10		39	**NC**
NC	11		38	**NC**
VCC	12		37	**VCC**
VSS	13		36	**VSS**
NC	14		35	**NC**
NC	15		34	**NC**
CLE	16		33	**NC**
ALE	17		32	**I/O3**
#WE	18		31	**I/O2**
#WP	19		30	**I/O1**
NC	20		29	**I/O0**
NC	21		28	**NC**
NC	22		27	**NC**
NC	23		26	**NC**
NC	24		25	**NC**

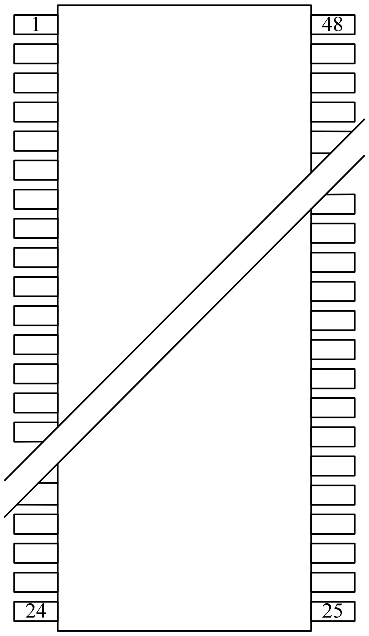

Figure 2:Device Organization

Table 1:Signal Descriptions

Name	Function
I/O0~I/O7	**DATA INPUTS/OUTPUTS** The I/O pins are used to input command, address and data, and to output data during read operations. The I/O pins float to high-z when the chip is deselected or when the outputs are disabled.
CLE	**COMMAND LATCH ENABLE** The CLE input controls the activating path for commands sent to the command register. When active high, commands are latched into the command register through the I/O ports on the rising edge of the WE signal.
#CE	**Chip Enable Input .**When #CE is Low, the command input cycle becomes valid. When #CE is High, all inputs are ignored.
ALE	**ADDRESS LATCH ENABLE** The ALE input controls the activating path for the address to the internal address registers. Addresses are latched on the rising edge of #WE with ALE high.
#RE	**READ ENABLE** The #REn input is the serial data-out control, and when active， drives the data onto the I/O bus. Data is valid tREA after the falling edge of #RE which also increments the internal column address counter by one.
#WE	**WRITE ENABLE** The #WEn input controls writes to the I/O port. Commands, address and data are latched on the rising edge of the #WE pulse.
#WP	**WRITE PROTECT** The #WP pin provides inadvertent write/erase protection during power transitions. The internal high voltage generator is reset when the #WP pin is active low.
#R/B	**READY/BUSY OUTPUT** The R/B output indicates the status of the device operation. When low it indicates that a program, erase or random read operation is in process and returns to high state upon completion. It is an open drain output and does not float to high-z condition when the chip is deselected or when outputs are disabled.
VCC	**POWER** VCC is the power supply for device.
VSS	**GROUND**

5. ELECTRICAL SPECIFICATIONS

5.1. Absolute Maximum Ratings

Table 2:Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Voltage input	V_{IN}	-0.6 to + 4.6	V
V_{CC} Supply voltage	V_{CC}	-0.6 to + 4.6	V
V_{CCQ} Supply voltage	V_{CCQ}	-0.6 to + 4.6	mA
Operating temperature	T_A	-55 to +125	℃
Storage temperature	T_{STG}	-65 to +150	℃

5.2. Recommended DC Operating Conditions

Table 3:Recommended DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
V_{CC} Supply voltage	V_{CC}	2.7	3.3	3.6	V
Input high voltage	V_{IH}	V_{CC}×0.8	——	V_{CC}+0.3	V
Input low voltage	V_{IL}	-0.3	——	0.2×V_{CC}	V

5.3. DC Characteristics And Operating Conditions

Table 4:DC And Operating Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input leakage current	ILI	Any input V_{IN} = 0V to V_{CC} (all other pins under test = 0V)	-	-	±10	uA
Output leakage current	ILO	DQ are disabled; V_{OUT} = 0V to V_{CC}	-	-	±10	uA

6. TYPICAL APPLICATION

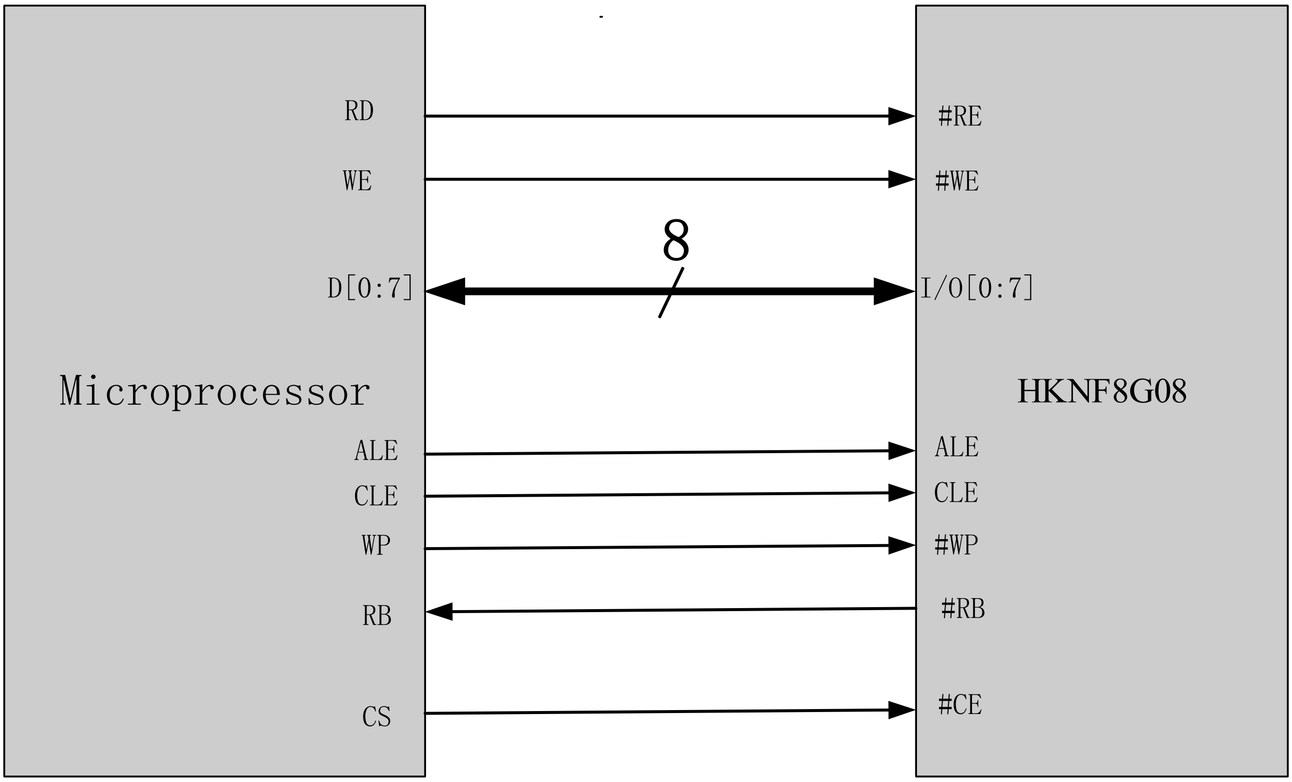

Figure 3:Typical Application

7. ORDERING INFORMATION

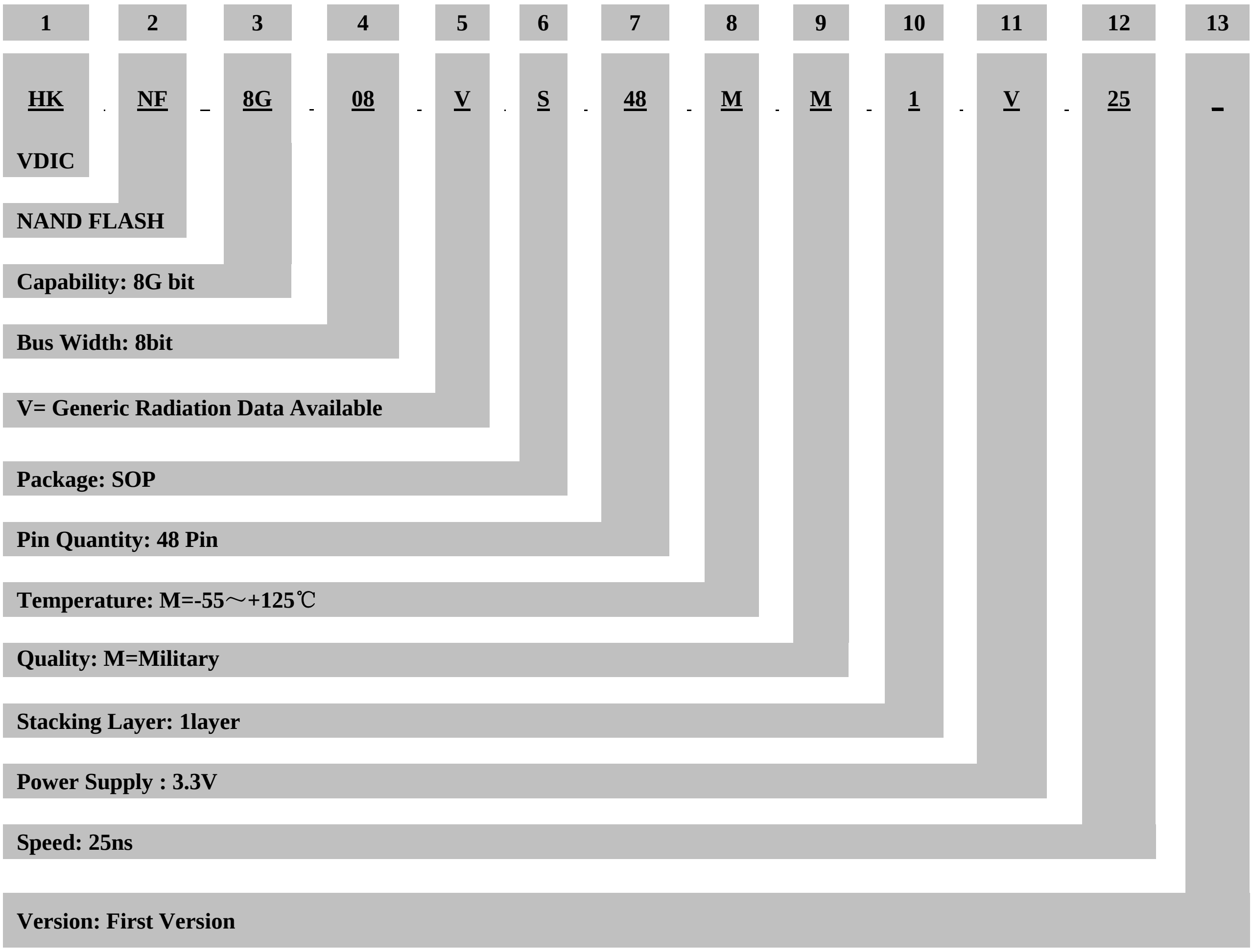

Table 5:Part Information

Part Number	Capacity (bit)	Bus Width (bit)	Radiation			Packaging	Temperature（℃）
			TID[1]	SEL[2]	SEU[3]		
HKNF8G08VS48MM1V25	8G	8	-	-	-	SOP48	-55 ～＋125

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[1] TID: Total Dose（Krads(Si)）

[2] SEL: LET Threshold（Mev.cm2/mg）

[3] SEU:SEU Threshold （Mev.cm2/mg）

8. PACKAGE DIMENSIONS

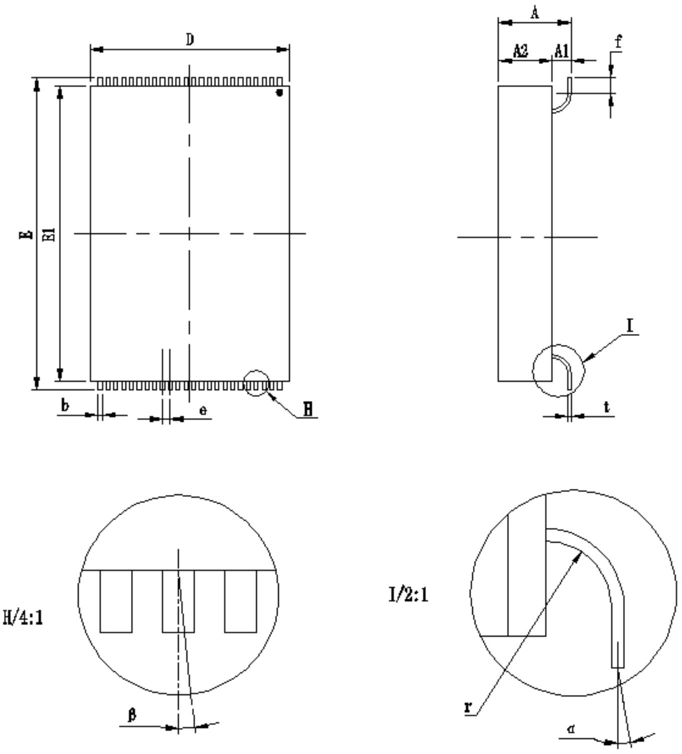

Figure 4 Package dimensions

Table 6 Dimensions information

	Min	Max
A	4.30	5.00
A2	3.10	3.70
D	12.70	13.10
E	19.80	20.20
E1	18.80	19.20
f	1.20	
b	0.25	
e	0.50	
r	1.00	
t	0.20	
α	≤3°	
β	≤3°	
NOTE: 1. Unit: mm 2. A1= A - A2		

9. REVISION HISTORY

Table 7 Revision history

Revision	Date	Description of Change
A0	Feb 1,2018	First Created