VDIC MAGNETORESISTIVES RANDOM ACCESS MEMORY

VDMR8M32XS68XX8V35 USER MANUAL

Version : B5

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Zhuhai Orbita Aerospace Science & Technology Co.，Ltd.
Add: Orbita Tech Park, NO.1 Baisha Road，Tangjia Dong ` an，
Zhuhai, *Guangdong,* China 519080
Tel: +86-756-3391979 Fax: +86-756-3391980

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VDIC-MRAM

HIGH-SPEED 3.3V 256K × 32bit

MAGNETORESISTIVES RANDOM ACCESS MEMORY

1. DESCRIPTION

The VDMR8M32XS68XX8V35 is a 8 × 1,048,576-bit high-speed access time, high-density Magnetoresistives Random Access Memory device. Manufactured with VDIC Very Dense SiP technology, this Die stacks eight 1-Mbit MRAM Dies. It is organized as eight independent dies of 128K x 8bit wide data interface.

The VDMR8M32XS68XX8V35 offers MRAM compatible 35ns read/write timing with unlimited endurance. Data is always non-volatile for greater than 20-years. Data is automatically protected on power loss by low-voltage inhibit circuitry to prevent writes with voltage out of specification. The VDMR8M32XS68XX8V35 is the ideal memory solution for applications that must permanently store and retrieve critical data and programs quickly.

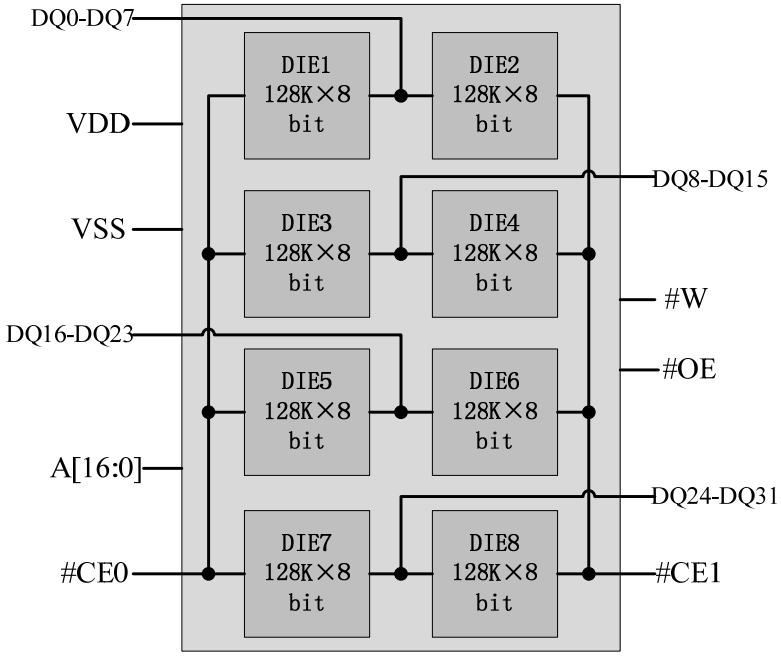
The VDMR8M32XS68XX8V35 has eight dies. Each die can be selected separately with dedicated #CEn. Low interconnect parasitic capacitance of the stacking technology, by reducing the connection length, allows this MRAM module to be useful for a variety of high bandwidth, high performance and high density memory system applications.

The VDMR8M32XS68XX8V35 is available in a 68-pin SOP package.

2. FEATURES

- Fast 35ns Read/Write Cycle
- SRAM Compatible Timing, Uses Existing SRAM Controllers Without Redesign
- Unlimited Read & Write Endurance
- Data Always Non-volatile for >20-years at storage temperature
- One Memory Replaces Flash, SRAM, EEPROM and BBSRAM in a system for simpler, more efficient design
- Stack of eight 1Mbit MRAM
- Organized as 8 dies of 128K x 8 bit memory
- Two independent Die Select
- 3.3 Volt Power Supply
- Automatic Data Protection on Power Loss
- -Industrial, Automotive Temperatures
- -68-lead SOP package

3. BLOCK DIAGRAM



(All other signals are common to the eight memories)

Figure 1 Block diagram

4. PIN DESCRIPTIONS

Pin Id	Pin #		Pin Id
DQ9	1	68	**DQ15**
DQ8	2	67	**DQ14**
DQ17	3	66	**DQ23**
DQ16	4	65	**DQ22**
#CE1	5	64	**DQ30**
NC	6	63	**DQ31**
DC	7	62	**DC**
NC	8	61	**NC**
A0	9	60	**DC**
A1	10	59	**DQ24**
A2	11	58	**DQ25**
A3	12	57	**A16**
A4	13	56	**A15**
#CE0	14	55	**#OE**
DQ0	15	54	**DQ7**
DQ1	16	53	**DQ6**
VDD	17	52	**VSS**
VSS	18	51	**VDD**
DQ2	19	50	**DQ5**
DQ3	20	49	**DQ4**
#W	21	48	**DC**
A5	22	47	**A14**
A6	23	46	**A13**
A7	24	45	**A12**
A8	25	44	**A11**
A9	26	43	**A10**
DC	27	42	**DC**
DC	28	41	**DC**
DQ27	29	40	**DQ28**
DQ26	30	39	**DQ29**
DQ19	31	38	**DQ21**
DQ18	32	37	**DQ20**
DQ11	33	36	**DQ13**
DQ10	34	35	**DQ12**

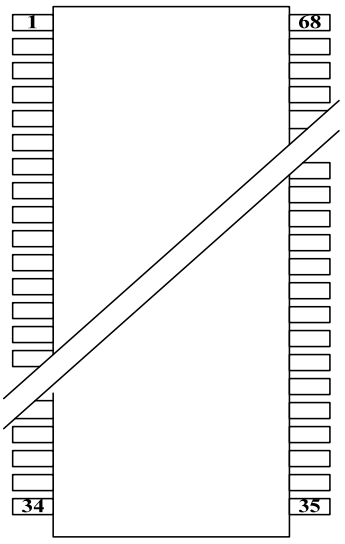


Figure 2 Pin configuration

Table 1 Pin description

Pin	Name	Function
#CE0	Die select	Disables or enables memory operation for die1,die3,die5 and die 7
#CE1	Die select	Disables or enables memory operation for die2,die4,die6 and die 8
A0 ~ A16	Address	17-bit addresses
#W	Write enable	Enables write operation common to all memory dies
#OE	Output enable	Enables data output common to all memory dies
DQ0~ DQ31	Data input/output	Data inputs/outputs 32-bit wide bus
VDD/VSS	Power supply/ground	Power and ground for the input/output buffers and core logic.
NC	No connection	These pins are recommended to be left No Connection on the device.
DC	Do not connect	These pins do not connect

5. ELECTRICAL SPECIFICATIONS

5.1. ABSOLUTE MAXIMUM RATINGS

This device contains circuitry to protect the inputs against damage caused by high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage greater than the maximum rated voltages to these high-impedance (Hi-Z) circuits.

The device also contains protection against external magnetic fields. Precautions should be taken to avoid application of any magnetic field more intense than the maximum field intensity specified in the maximum ratings.

Table 2 Absolute maximum ratings

Characteristics	Symbol	Maximum ratings	Unit	Remarks
Voltage on V_{DD} supply relative to Vss	V_{DD}	-0.5 ~ +4.0	V	——
Voltage on any pin relative to Vss	V_{IN}	-0.5 ~ VDD +0.5	V	——
Operating Temperature Range	T_{OPR}	-55 ~ +95	℃	——
Storage Temperature Range	T_{STG}	-55 ~ +125	℃	——
Power Dissipation	P_D	< 1.0	W	——
Junction Temperature	T_J	150	℃	
Maximum Body Temperature (short exposure only)	T_{MAX}	215	℃	Measured at module side level (exposure < 60s)

5.2. RECOMMENDED DC OPERATING CONDITIONS

Table 3 Recommended DC operating condition

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{DD}	3.0	3.3	3.6	V

Parameter	Symbol	Min	Typ	Max	Unit
Input voltage	V_{IH}	2.2	——	V_{DD}+0.3	V
	V_{IL}	-0.5	——	0.8	V
Write inhibit voltage	V_{WI}	2.5	2.7	3.0	V

5.3. DC ELECTRICAL CHARACTERISTICS

Table 4 DC electrical characteristics

Parameters	Symbol	Test Conditions	Min	Max	Unit
Output voltage low level	V_{OL}	V_{DD} =3.0V,I_{OL}= +4mA	——	0.4	V
Output voltage high level	V_{OH}	V_{DD} =3.0V,I_{OL}= -4mA	2.4	——	V

5.4. MODULE CAPACITANCE

For the MRAM module VDMR8M32xS68xx8V35, the capacitance values are:

(TA = 25℃, f = 1.0MHz, VPP = 0.1V)

Table 5 Pin Capacitance

Parameters	Symbol	Min	Max	Unit
Input Capacitance (#CE[0:1], #W, #OE)	C_{IN}	——	55	pF
Input Capacitance	C_{IN1}	——	55	pF
I/O Capacitance	$C_{I/O}$	——	20	pF

6. TYPICAL APPLICATION

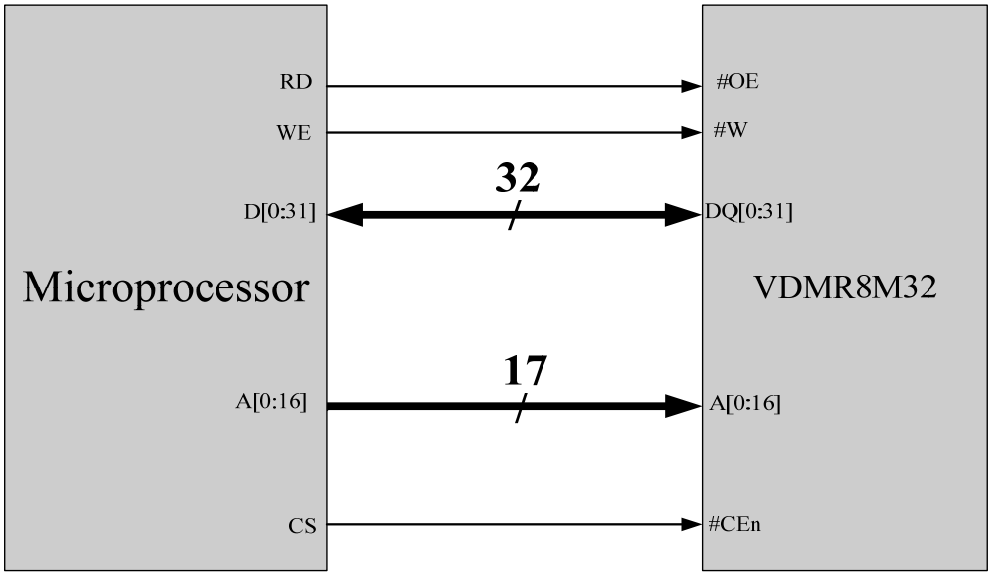


Figure 3 Typical application

7. ORDERING INFORMATION

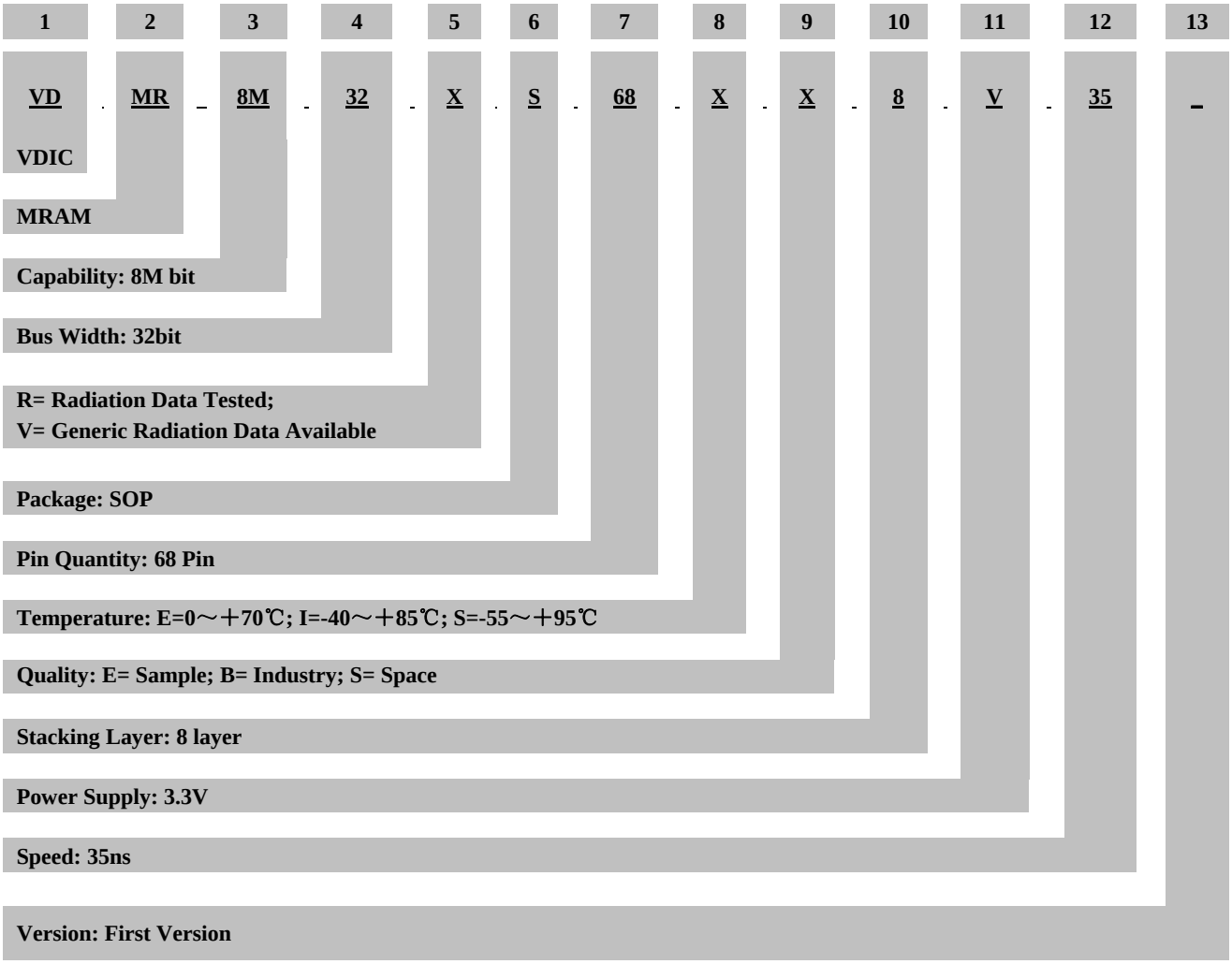


Table 6 Ordering information

Part Number	Capacity (bit)	Bus Width (bit)	Radiation			Packaging	Temperature (℃)
			TID[1]	SEL[2]	SEU[3]		
VDMR8M32VS68EE8V35	8M	32	-	-	-	SOP68	0 ~ + 70
VDMR8M32VS68IB8V35	8M	32	-	-	-	SOP68	-40 ~ + 85
VDMR8M32RS68SS8V35	8M	32	> 50	> 80.3	< 14.2, > 9.3	SOP68	-55 ~ + 95

[1] TID: Total Dose（Krads(Si)）
[2] SEL: LET Threshold（Mev.cm2/mg）
[3] SEU:SEU Threshold （Mev.cm2/mg）

8. PACKAGE DIMENSIONS

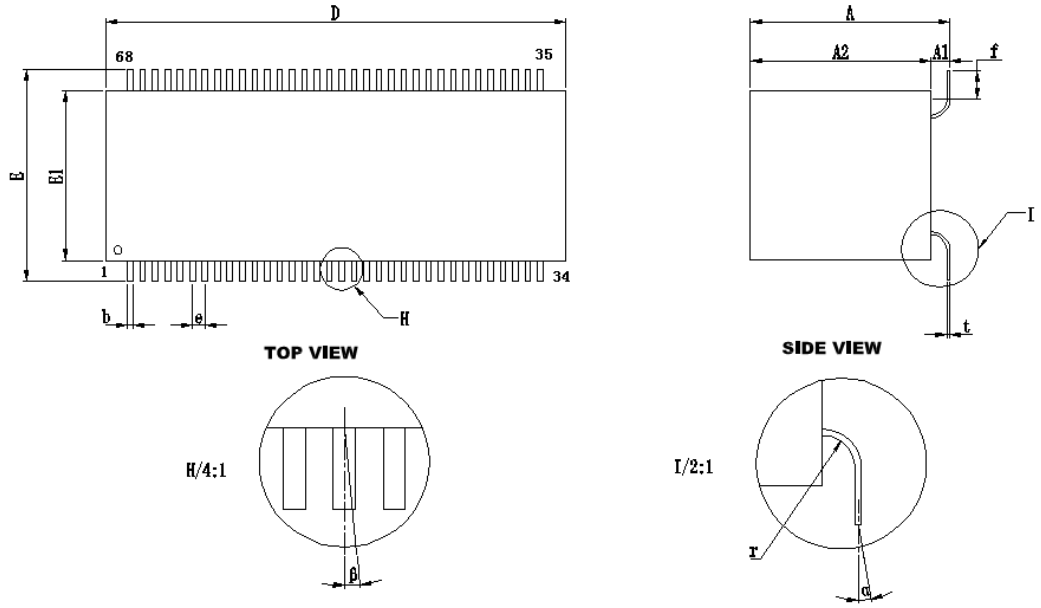


Figure 4 Package dimensions

Table 7 Dimensions information

	Min	Typical	Max
A	12.60	—	13.20
A2	11.40	—	11.90
D	29.50	—	29.90
E	13.40	—	13.80
E1	10.80	—	11.20
f	1.80	—	2.20
b	0.32	—	0.38
e	—	0.8	—
r	1.00	—	1.20
t	0.18	—	0.22
α	—	—	3°
β	—	—	3°
NOTE: 1.Uint: mm 2. A1= A - A2			

9. PADS DESIGNATION

It is highly recommended to design pads as below.

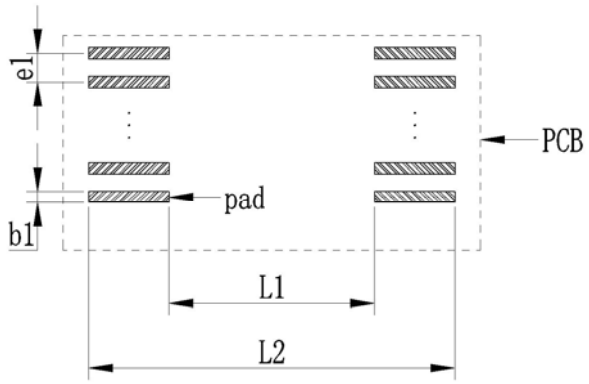


Figure 5 Pads Dimensions

NOTE:

e1: 0.8 mm;

b1: 0.5mm;

L1: 6.4mm;

L2: 14.8mm.

10. REVISION HISTORY

Table 8 Revision history

Revision	Date	Description of Change
A0	Nov 3,2015	First Created
A1	Mar 14,2016	Modified the PIN DESCRIPTIONS
A2	Aug 23,2016	Modified the ORDERING INFORMATION
A3	Jan 9,2017	Modified the PACKAGE DIMENSIONS
A4	Oct.25,2017	Changed company's name to Zhuhai Orbita Aerospace Science & Technology Co. , Ltd
A5	Mar 13,2018	Add or reduce the chapters
B0	May 22, 2018	Modified Operating Temperature Range and Storage temperature.
B1	Mar 21,2020	Update TID and SEE
B2	Feb 22, 2021	Update TID and SEE
B3	April 22nd, 2021	Add pads designation
B4	Jun 15, 2021	Add maximum body temperature
B5	Jun 22, 2021	Add pin capacitance