# VDIC ASYNCHRONOUS STATIC RAM

# VDSR4M08XS44XX1V12 USER MANUAL

**Version : B0**

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# Contents

# VDIC-SRAM

## HIGH-SPEED 3.3V 512K × 8 bit

## ASYNCHRONOUS STATIC RAM

## 1 Description

The VDSR4M08XS44XX1V12 is a high-speed access time, high-density Static Random Access Memory with 4Mbit. Manufactured with VDIC Very Dense SIP technology, this block is stacked by one SRAM die employing CMOS process. It is organized as 512K×8bit wide data interface .The block can be selected separately with dedicated #CE.

Low interconnect parasitic capacitance of the stacking technology, by reducing the connection length, allows this SRAM module to be useful for a variety of high bandwidth, high performance and high density memory system applications.

The VDSR4M08XS44XX1V12 is available in a 44-pin SOP package.

## 2 Features

- High-speed access time: 12ns
- TTL compatible inputs and outputs
- Operating voltage range: 2.7 V to 3.6 V
- Error indication (ERR) pin to indicate 1-bit error detection and correction
- Low active and standby currents

  Active current: $I_{CC}$= 38 mA typical

  Standby current: $I_{SB2}$ = 6 mA typical

## 3 Block Diagram

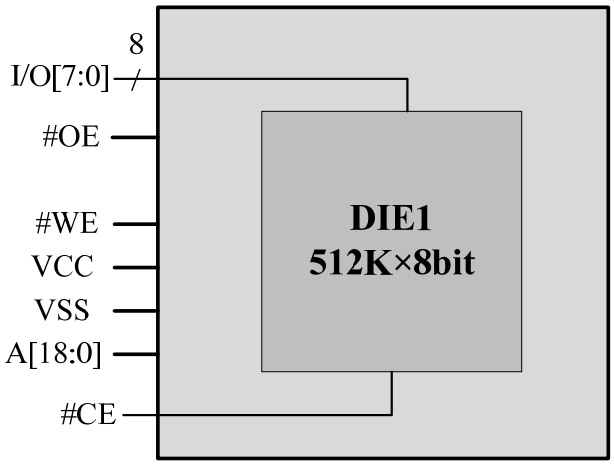


Figure 1: Block diagram

# 4 Pin Descriptions

| Pin Id | Pin # | | Pin Id |
|---|---|---|---|
| **NC** | 1 | 44 | **NC** |
| **NC** | 2 | 43 | **NC** |
| **A0** | 3 | 42 | **NC** |
| **A1** | 4 | 41 | **A18** |
| **A2** | 5 | 40 | **A17** |
| **A3** | 6 | 39 | **A16** |
| **A4** | 7 | 38 | **A15** |
| **#CE** | 8 | 37 | **#OE** |
| **I/O0** | 9 | 36 | **I/O7** |
| **I/O1** | 10 | 35 | **I/O6** |
| **VCC** | 11 | 34 | **VSS** |
| **VSS** | 12 | 33 | **VCC** |
| **I/O2** | 13 | 32 | **I/O5** |
| **I/O3** | 14 | 31 | **I/O4** |
| **#WE** | 15 | 30 | **A14** |
| **A5** | 16 | 29 | **A13** |
| **A6** | 17 | 28 | **A12** |
| **A7** | 18 | 27 | **A11** |
| **A8** | 19 | 26 | **A10** |
| **A9** | 20 | 25 | **NC** |
| **NC** | 21 | 24 | **NC** |
| **NC** | 22 | 23 | **NC** |

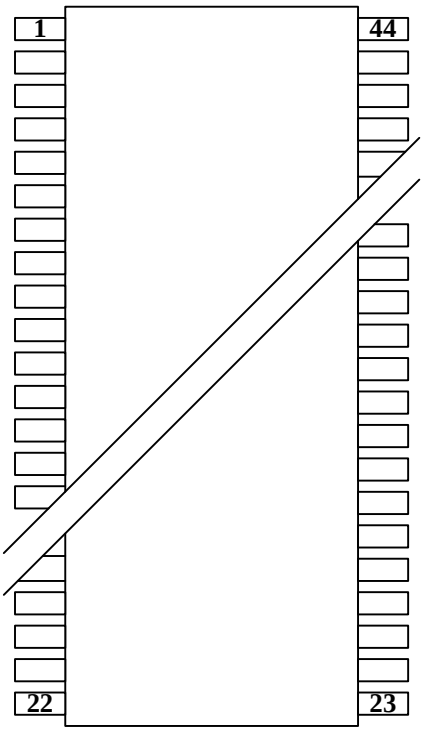


Figure 1 Pin configuration

**Table 1 Pin description**

| Pin | Name | Function |
|---|---|---|
| #CE | Block select | Chip Enable Input |
| A0 ~ A18 | Address | Address Inputs |
| #WE | Write enable | Write Enable Input |
| #OE | Output enable | Output Enable Input |
| I/O0~I/O7 | Data input/output | Data inputs/outputs 8-bit wide bus |
| VCC/VSS | Power supply/ground | Power and ground for the input/output buffers and core logic. |
| NC | No connection | This pin is recommended to be left No Connection on the device. |

# 5 Command Operation

## 5.1 DC Electrical Characteristics

**Table 2 Absolute maximum ratings**

| Parameter | Symbol | Maximum ratings | Unit |
|---|---|---|---|
| Voltage on $V_{CC}$ supply relative to $V_{SS}$ | $V_{CC}$ | -0.5 to $V_{CC}$+0.5 | V |
| Voltage on any pin relative to $V_{SS}$ | $V_{IN}$ | -0.5 to $V_{CC}$+0.5 | V |
| Power Dissipation | $P_D$ | <0.5 | W |
| Thermal Resistance Junction to Case | $R_{J-C}$ | <20 | ℃/W |
| Manual Soldering Temperature Range | $T_M$ | +250 ~ +280 | ℃ |
| Reflow Soldering Temperature | $T_{SOL}$ | 215 | ℃ |
| Operating Temperature Range | $T_{OPR}$ | -55 to +125 | ℃ |
| Storage Temperature Range | $T_{STG}$ | -65 to +150 | ℃ |

## 5.2 Absolute Maximum Ratings

**Table 3 Recommended DC operating condition**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Supply voltage | $V_{CC}$ | 2.7 | 3.3 | 3.6 | V |
| Input high voltage | $V_{IH}$ | 2.0 | —— | $V_{CC}$+0.3 | V |
| Input low voltage | $V_{IL}$ | -0.3 | —— | 0.8 | V |

## 5.3 Recommended DC Operating Conditions

**Table 4 DC characteristics**

| Parameter | Symbol | TEST CONDITIONS | Min | Max | Unit |
|---|---|---|---|---|---|
| Output voltage low level | $V_{OL}$ | $V_{CC}$=2.7V，$I_{OL}$= 4mA | —— | 0.4 | V |
| Output voltage high level | $V_{OH}$ | $V_{CC}$=2.7V, $I_{OH}$= -1mA | 2.4 | —— | V |

# 6 TYPICAL APPLICATION

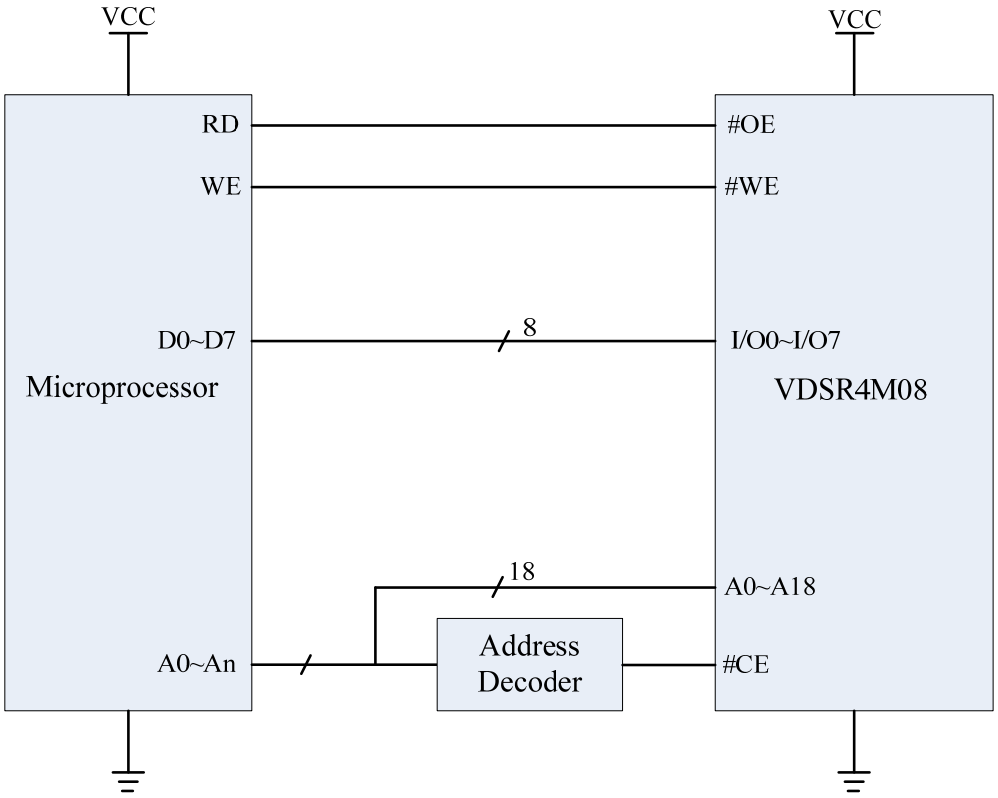


Figure 2 Typical application

# 7 Ordering Information

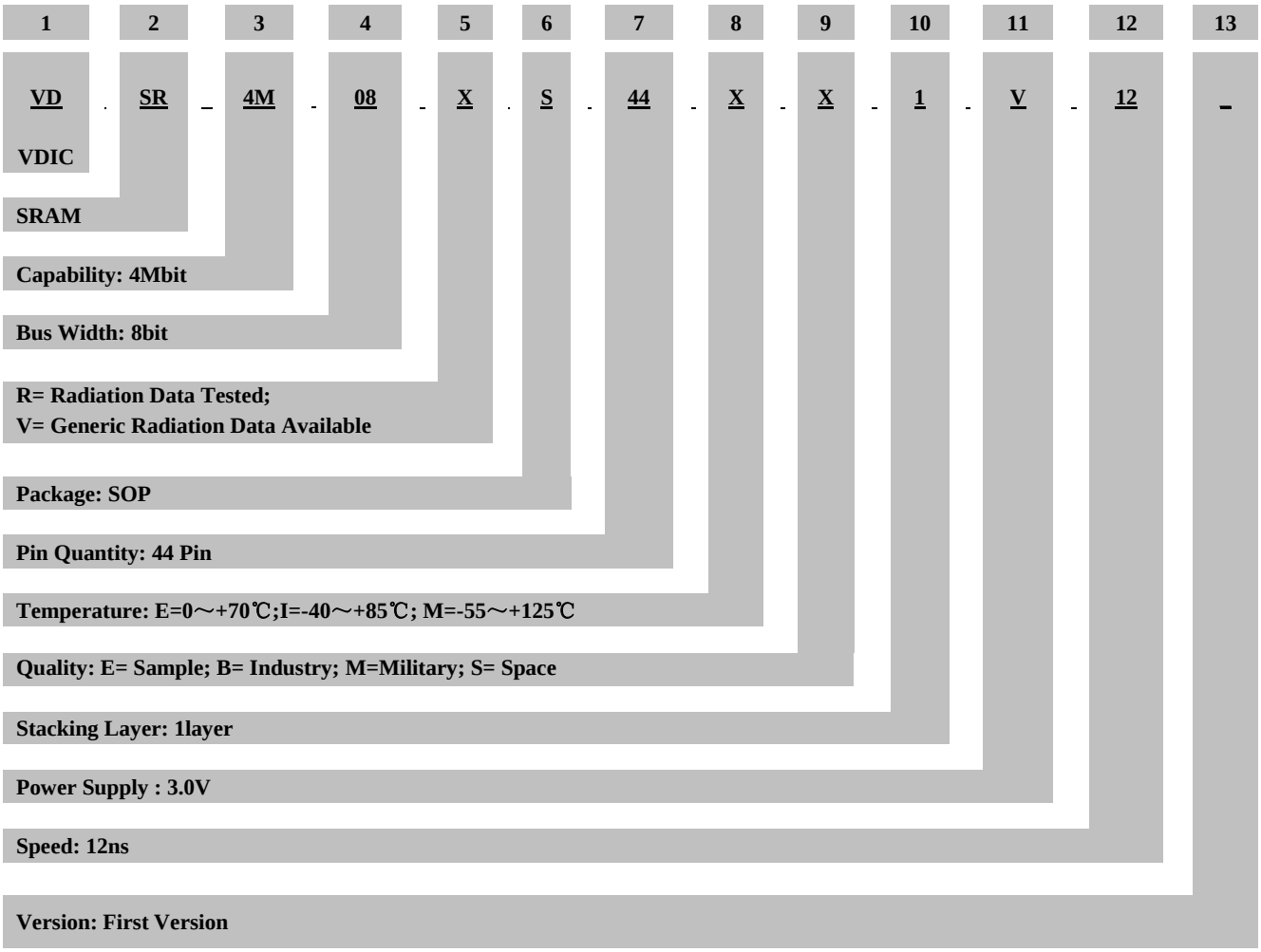


**Table 5 Ordering information**

| Part Number | Capacity (bit) | Bus Width (bit) | Radiation | | | Packaging | Temperature (℃) |
|---|---|---|---|---|---|---|---|
| | | | TID[1] | SEL[2] | SEU[3] | | |
| VDSR4M08VS44EE1V12 | 4M | 8 | - | - | - | SOP44 | 0 ~ +70 |
| VDSR4M08VS44IB1V12 | 4M | 8 | - | - | - | SOP44 | -40 ~ +85 |
| VDSR4M08VS44MM1V12 | 4M | 8 | - | - | - | SOP44 | -55 ~ +125 |
| VDSR4M08RS44MS1V12 | 4M | 8 | >100 | >27 | >0.2 | SOP44 | -55 ~ +125 |

[1] TID: Total Dose（Krads(Si)）
[2] SEL: LET Threshold（Mev.cm2/mg）
[3] SEU:SEU Threshold （Mev.cm2/mg）

# 8 Package Dimensions

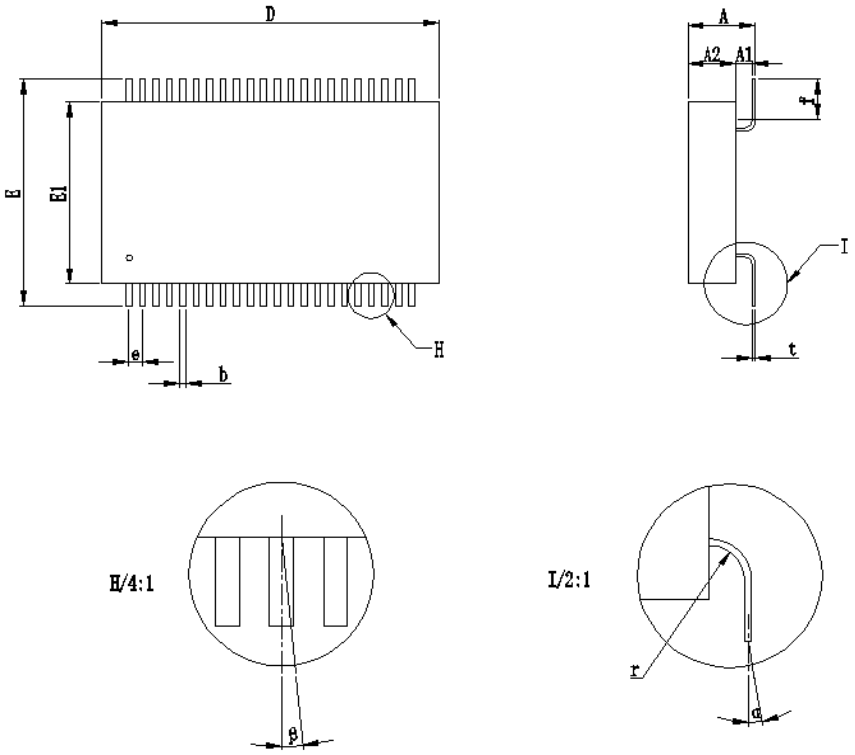


Figure 3 Package dimensions

**Table 6 Dimensions information**

| | Min | Max |
|---|---|---|
| A | 3.70 | 4.40 |
| A2 | 2.50 | 3.10 |
| D | 19.80 | 20.20 |
| E | 13.40 | 13.80 |
| E1 | 10.80 | 11.20 |
| f | 2.00 | |
| b | 0.35 | |
| e | 0.80 | |
| r | 1.00 | |
| t | 0.20 | |
| α | ≤3° | |
| β | ≤3° | |
| NOTE: 1. Unit: mm<br>2. A1= A – A2 | | |

# 9 REVISION HISTORY

**Table 7 Revision history**

| Revision | Date | Description of Change |
|---|---|---|
| A0 | Aug 10,2018 | First Created |
| A1 | Feb 21,2019 | Change Features and Command Operation |
| A2 | Apr 15,2019 | Change Features |
| A3 | May 15,2019 | Change Features and Command operation |
| B0 | Mar 21,2020 | Update TID and SEE |