OCE PROM MEMORY User Manual

OCE28V256X User's Manual

2017-UM-013

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OCE28V256X User's Manual

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User Manual

1. DESCRIPTION

OCE28V256X is a single voltage (3.3V), asynchronous, rad - hard 32kbit x8 memory device using anti - fuse based One-Time Programmable (OTP) memory cells. A standard 1 30nm CMOS process has been used to implement OCE28V256X with a dedicated robust Rad -Hard By Design (RHBD) approach. OCE28V256X has been specifically designed for hostile environments. A dual matrix topology guarantees safer reading margin and better resiliency to single events.

2. FEATURES

- A synchronous rad- hard 32k bit x8 OTP memory
- Operating Voltage (I/O) 3.3V±10%
- Programming voltage 5V
- 30ns max address access time
- Wide Temperature Range: -55°C to +125°C
- RC28F256 A R H uses IHP SG13S process
- Max Power Consumption:
  1. Core: 20mW @ 30MHz (READ)
  2. Core: 60mW (WRITE)
  3. Core: 50u W (Stand - by)
  4. I/O: 1mW @30MHz (READ)
  5. I/O : 2mW (WRITE)
  6. I/O : 0.3mW (Stand- by)
- Radiation Hardened process and design:
  1. Total Dose > 1 Mrad(Si)
  2. SEL LETth > 8 0 MeV cm/mg
  3. SEU LETth < 6 MeV cm/mg
- Packaging options:
  1. no package (waffle pack die)
  2. 28- Lead Flatpack
  3. 28- Lead CERDIP (only for evaluation)
  4. Embedded macro

3. BLOCK DIAGRAM

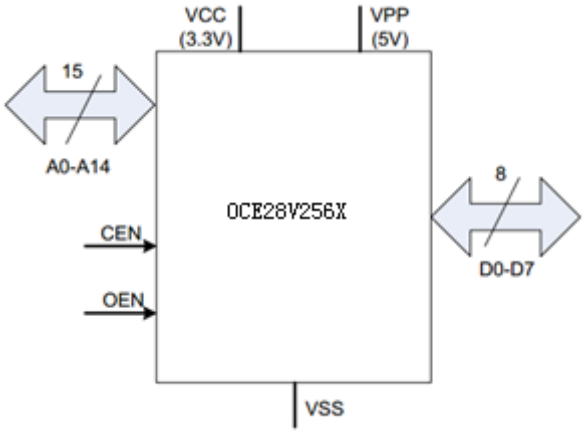


Figure 1 –PROM Block Diagram

4. DEVICE OPERATION

The OCE28V256X has three control inputs: Chip Enable (#CE), Program Enable (#PE), and Output Enable (#OE); fifteen address inputs, A(14:0); and eight bidirectional data lines, DQ(7:0). #CE is the device enable input that controls chip selection, active, and standby modes. Asserting #CE causes IDD to rise to its active value and decodes the fifteen address inputs to select one of 32,768 words in the memory. #PE controls program and read operations. During a read cycle, OE must be asserted to enable the outputs.

#OE	VPP[1]	#CE	I/O MODE	MODE
X	X	H	Three-state	Standby
L	L	L	Data Out	Read
H	H	L	Data In	Program
H	L	L	Three-state	Output Disable

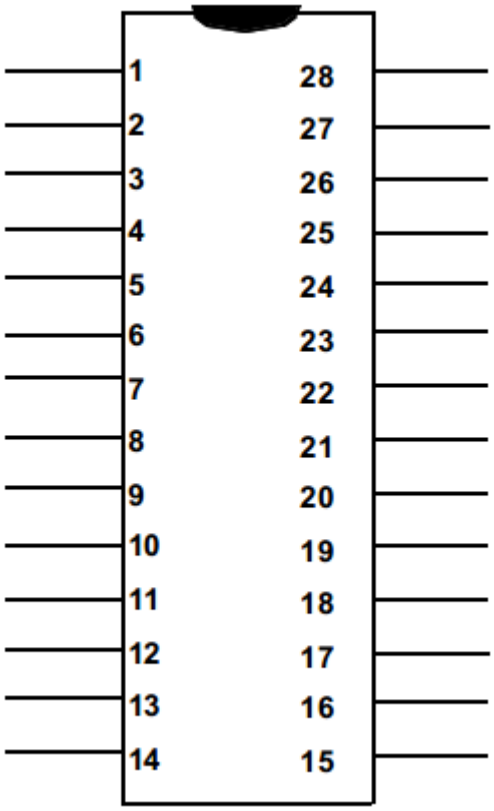
Table 1. Device Operation Truth Table[2]

[1] VPP can assume a High voltage (5V) during programming and a Low voltage (3.3V) during reading.
[2] "X" is defined as a "don't care" condition.

5. PIN ASSIGNEMENT

Symbol	Pin#		Pin#	Symbol
A14	**1**		**28**	V_{CC}
A12	**2**		**27**	V_{PP}
A7	**3**		**26**	A13
A6	**4**		**25**	A8
A5	**5**		**24**	A9
A4	**6**		**23**	A11
A3	**7**		**22**	#OE
A2	**8**		**21**	A10
A1	**9**		**20**	#CE
A0	**10**		**19**	DQ7
DQ0	**11**		**18**	DQ6
DQ1	**12**		**17**	DQ5
DQ2	**13**		**16**	DQ4
V_{SS}	**14**		**15**	DQ3

Table 2– Pin Assignment



Top view

6. PIN DESCRIPTION

Pin	Name
#CE	Chip Enable
#OE	Output Enable
V_{PP}	Programming Voltage
A0 ~ A14	Address
DQ0~ DQ7	Data input/output
V_{CC}/V_{SS}	Power supply (I/O) /ground

Table 3 – Pin Description

7. ELECTRICALSPECIFICATIONS

7.1. ABSOLUTEMAXIMUMRATINGS

Parameter	Symbol	Value	Unit
DC supply voltage	V_{cc}	- 0.5 to 4.6	V

Voltage on any pin	$V_{I/O}$	- 0.5 to 4.6	V
Power Dissipation	P_D	0.7	W
Thermal resistance Junction to case	R_{J-C}	3	°C/W
DC input current	I_I	±10	mA
Operating temperature	T_A	E：0~ +70 M: -55~ +125 S：-55~ +125	°C
Storage temperature	T_{STG}	-65 to +150	°C

Table 4 –Absolute Maximum Ratings

7.2. Recommended DC Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit
Supply voltage	V_{cc}	3.0	—	3.6	V
Programming Voltage	V_{PP}	—	5.0	—	V
Case temperature range	T_C	-55	—	+125	°C
High-level input voltage	V_{IH}	V_{CC}-0.9	—	V_{CC}+0.9	V
Low-level input voltage	V_{IL}	-0.9	—	0.9	V

Table 5 - Recommended DC Operating Conditions

8. READ AND WRITE CYCLE

8.1. AC CHARACTERISTICS

Write Cycle

Symbol	Parameter		Unit	Value
t_{AVAW}	Write and verify cycle time	30	ms	min
t_{AVWL}	Address set- up time	10	ms	min
t_{AVWH}	Address valid to end of write	25	ms	min
t_{DVWH}	Data hold - up time	15	ms	min
t_{DVSU}	Data set- up time	0	ms	min
t_{ELWH}	Chip Select low to write end	5	ms	min
t_{WLWH}	Write pulse width	15	ms	min
t_{WHAX}	Address hold from end of verify	5	ms	min
t_{WHDX}	Data hold time	0	ms	min
t_{SC}	VPP high from enable high	2.5	ms	max
t_{HC}	VPP low from enable low	2.5	ms	min

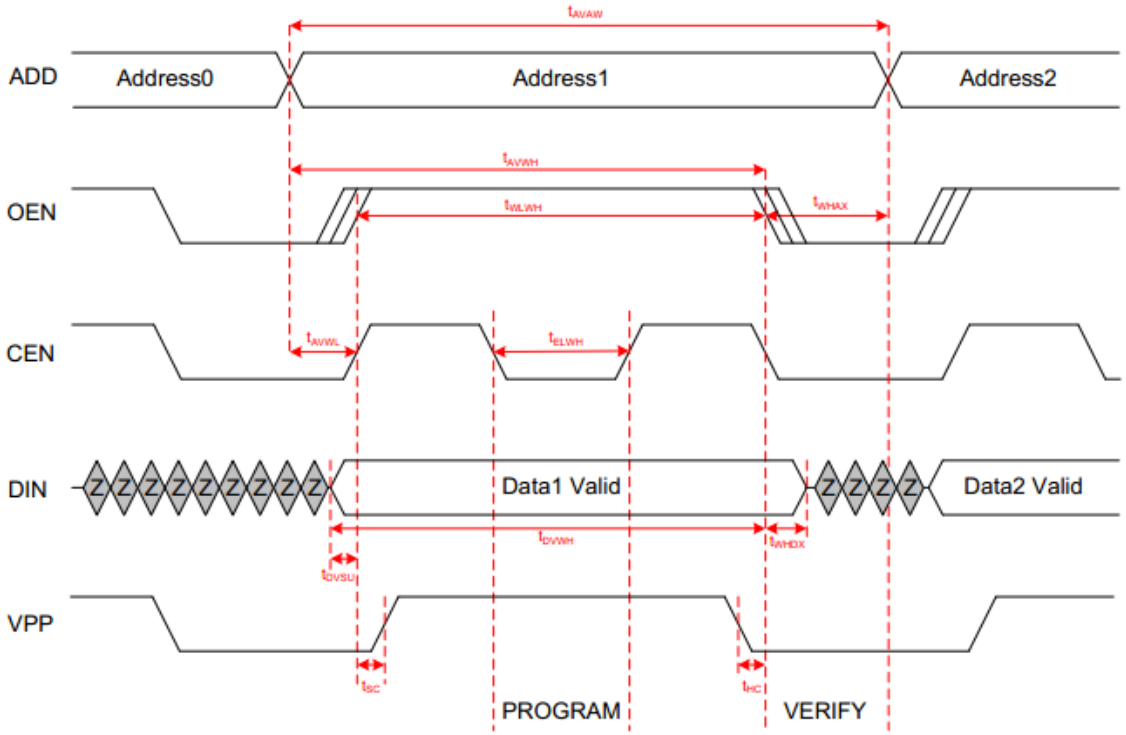


Figure 2- Write Cycle. Chip Enable Controlled

Read Cycle

Symbol	Parameter		Unit	Value
t_{AVAV}	Read cycle time	50	ns	min
t_{AVQV}	Read access time	30	ns	max
t_{AXQX}	Output hold time	0	ns	min
t_{AVGL}	Address valid to OEN low	tbd	ns	max
t_{GLQX}	Read access time (OEN)	30	ns	min
t_{ELGL}	CEN low to OEN low	tbd	ns	min
t_{GHEH}	OEN high to CEN high	tbd	ns	min
t_{GHAV}	OEN high to end of cycle	tbd	ns	min
t_{GHQZ}	#OE-controlled output three-state time	2	ns	min
t_{AVEL}	Address valid to CEN low	tbd	ns	min
t_{ELQX}	#CE-controlled output enable time	30	ns	min
t_{GLEL}	OEN low to CEN low	tbd	ns	min
t_{EHGH}	CEN high to OEN high	tbd	ns	min
t_{EHAV}	CEN high to end of cycle	tbd	ns	min
t_{EHQZ}	#CE-controlled output three-state time	2	ns	min

Table 6 - ACCharacteristics

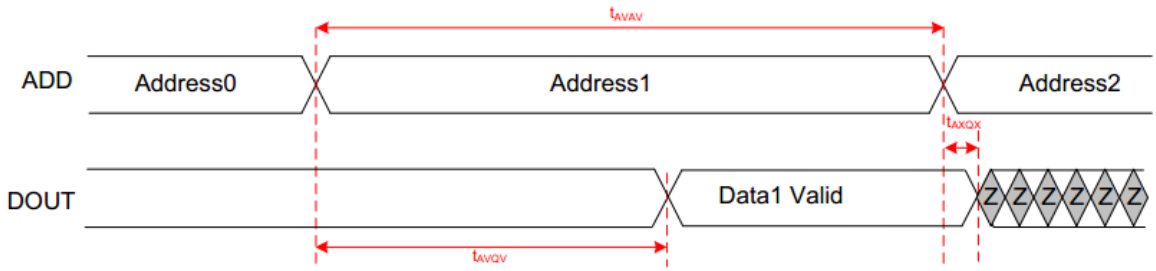


Figure 3-Read Cycle 1. Address Controlled

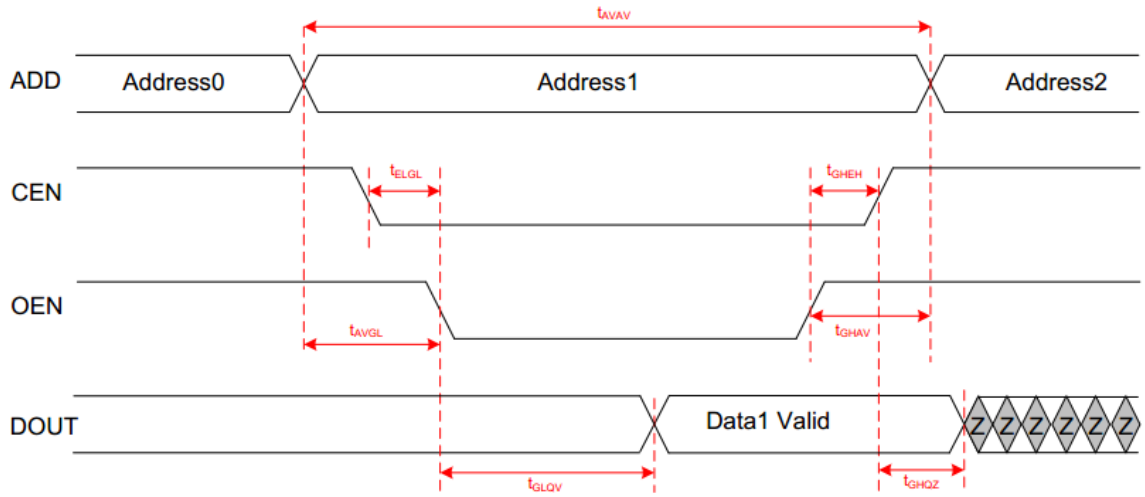


Figure 4-Read Cycle 2. Output Select Controlled

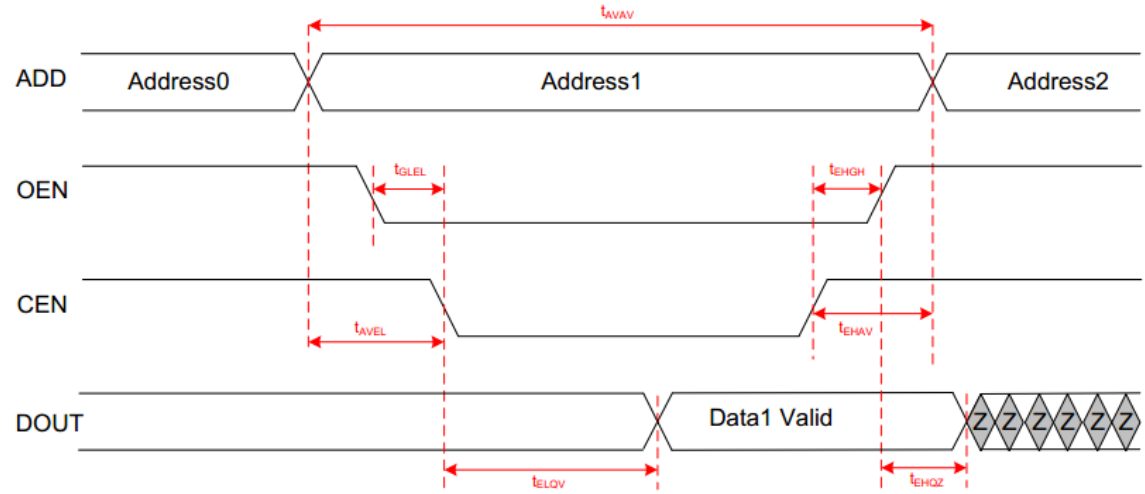


Figure 5- Read Cycle 3. Chip Enable Controlled

9. ORDERING INFORMATION

Part numbering:

1	2	3
OCE	**28V256**	**E**

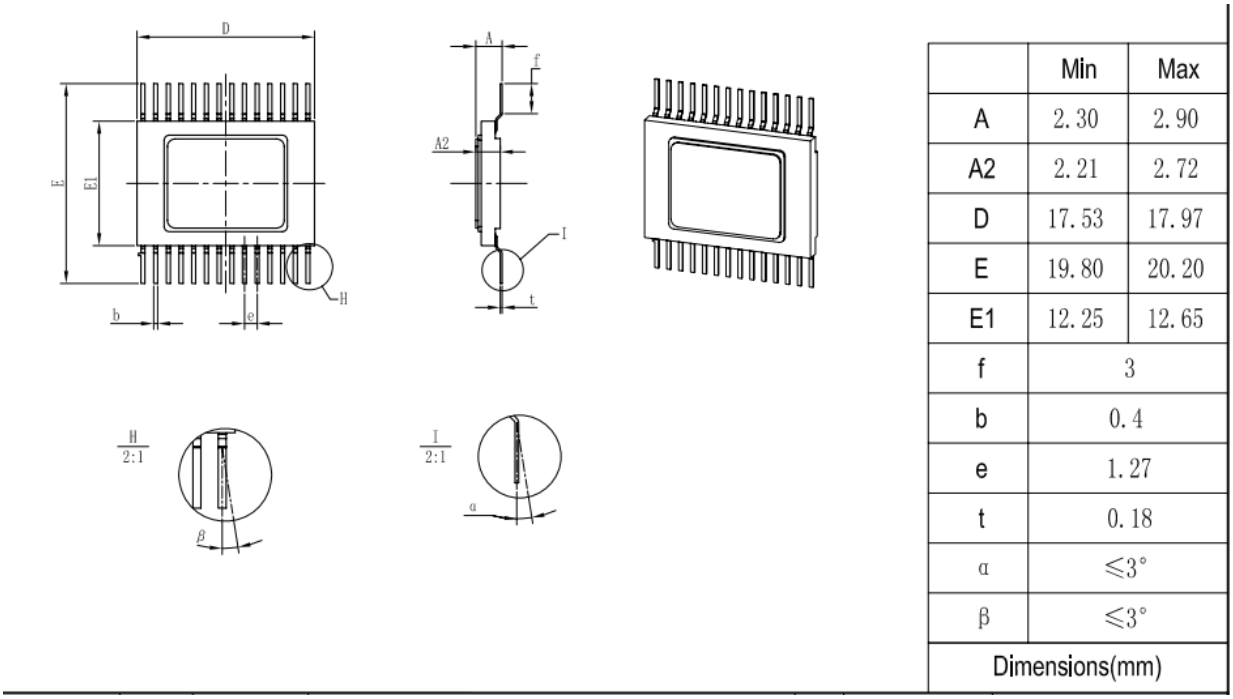
28V256:32Kx8 One Time Programmable PROM

Quality:
E= Sample, 0～70℃，Generic Radiation Data Available；
M= Military, -55~+125℃，Generic Radiation Data Available ;
S= Space,-55~+125℃，Radiation Data Tested.

Part Number	Capacity (bit)	Radiation			Bus Width (bit)	Temp range (℃)	Quality Flow
		TID[3]	SEL[4]	SEU[5]			
OCE28V256E	256k	-	-	-	8	0~+70	Sample
OCE28V256M	256k	-	-	-	8	-55~+125	Military
OCE28V256S	256k	>1	>80	<6	8	-55~+125	Space

Table 7 –Part numbers

10. PACKAGE TYPE AND DIMENSIONS



	Min	Max
A	2.30	2.90
A2	2.21	2.72
D	17.53	17.97
E	19.80	20.20
E1	12.25	12.65
f	3	
b	0.4	
e	1.27	
t	0.18	
α	≤3°	
β	≤3°	
Dimensions(mm)		

Figure 6–Mechanical outlines

[3] TID: Total Dose（Mrads(Si)）
[4] SEL:LET Threshold（Mev.cm2/mg (Si)）
[5] SEU:SEU Threshold（Mev.cm2/mg (Si)）

11. REVISIONHISTORY

Revision	Date	Description of Change
A0	Jun,11,2018	First created.

Table 8 –Revision history