

OCE PROM MEMORY User Manual

OCE28F256X User's Manual



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OCE28F256X User's Manual

DocumentRevision : OCE-2017-UM-013

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1. DESCRIPTION

The OCE28F256X amorphous silicon anti-fuse PROM is a high performance, asynchronous, radiation-hardened, 32K x 8 programmable memory device. The OCE28F256X PROM features fully asynchronous operation requiring no external clocks or timing strobes. An advanced radiation-hardened twin-well CMOS process technology is used to implement the OCE28F256X. The combination of radiation-hardness, fast access time, and low power consumption make the OCE28F256X ideal for high speed systems designed for operation in radiation environments.

2. FEATURES

- Programmable, read-only, asynchronous, radiation-hardened, 32K x 8 memory
 - Supported by industry standard programmer
- 45ns and 40ns maximum address access time (-55 °C to 125°C)
- TTL compatible input and TTL/CMOS compatible output levels
- Three-state data bus
- Low operating and standby current
 - Operating: 125mA maximum @25MHz
 - Standby: 2mA maximum
- VDD: 5.0 volts + 10%
- Radiation-hardened process and design; total dose irradiation testing to MIL-STD-883, Method 1019
 - Total dose: 1E5 rad(Si)
 - SUE: > 37.3MeV-cm²/mg
 - SEL: > 75 MeV-cm²/mg
 - AC and DC testing at factory
- Packaging options:
 - 28-lead 50-mil center flatpack (0.490 x 0.74)

3. BLOCK DIAGRAM

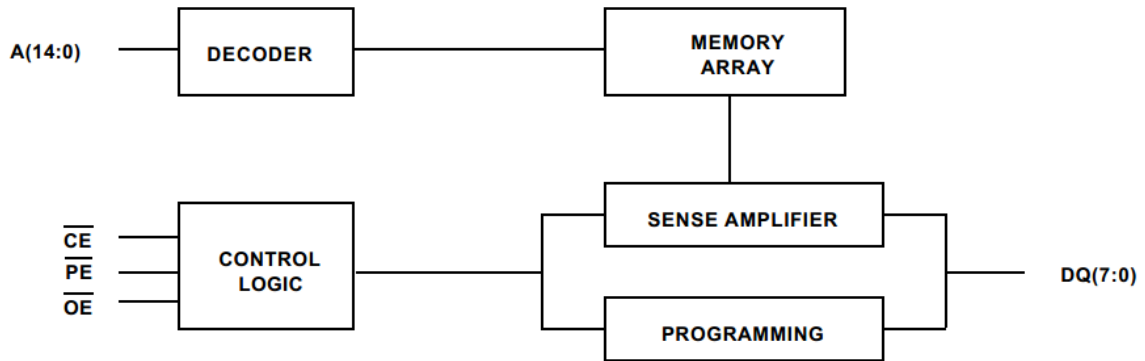


Figure 1 –PROM Block Diagram

4. DEVICE OPERATION

The OCE28F256X has three control inputs: Chip Enable ($\#CE$), Program Enable ($\#PE$), and Output Enable ($\#OE$); fifteen address inputs, A(14:0); and eight bidirectional data lines, DQ(7:0). $\#CE$ is the device enable input that controls chip selection, active, and standby modes. Asserting $\#CE$ causes I_{DD} to rise to its active value and decodes the fifteen address inputs to select one of 32,768 words in the memory. $\#PE$ controls program and read operations. During a read cycle, OE must be asserted to enable the outputs.

$\#OE$	$\#PE$	$\#CE$	I/O MODE	MODE
X	1	1	Three-state	Standby
0	1	0	Data Out	Read
1	0	0	Data In	Program
1	1	0	Three-state	Read ¹

Table 1. Device Operation Truth Table²

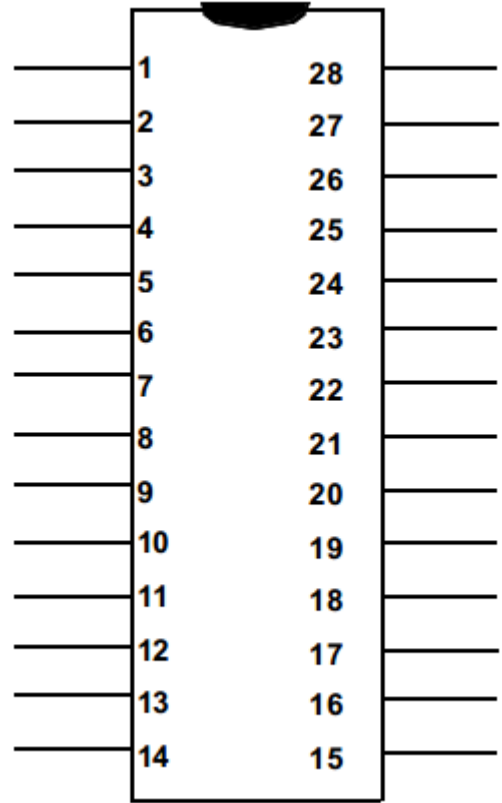
¹ Device active; outputs disabled.

² "X" is defined as a "don't care" condition.

5. PIN ASSIGNMENT

Symbol	Pin#	Pin#	Symbol
A14	1	28	V _{DD}
A12	2	27	#PE
A7	3	26	A13
A6	4	25	A8
A5	5	24	A9
A4	6	23	A11
A3	7	22	#OE
A2	8	21	A10
A1	9	20	#CE
A0	10	19	DQ7
DQ0	11	18	DQ6
DQ1	12	17	DQ5
DQ2	13	16	DQ4
V _{SS}	14	15	DQ3

Table 2– Pin Assignment



Top view

6. PIN DESCRIPTION

Pin	Name
#CE	Chip Enable
#OE	Output Enable
#PE	Program Enable
A0 ~ A14	Address
DQ0~ DQ7	Data input/output
V _{DD} /V _{SS}	Power supply/ground

Table 3 – Pin Description

7. ELECTRICAL SPECIFICATIONS

7.1. ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
DC supply voltage	V _{DD}	-0.3 to +7.0	V
Voltage on any pin	V _{I/O}	-0.5 to (V _{DD} + 0.5)	V
Power Dissipation	P _D	1.5	W

Thermal resistance Junction to case	R _J	3.3	°C/W
DC input current	I _I	±10	mA
Operating temperature	T _A	E: 0~ +70 S: -55~ +125	°C
Storage temperature	T _{STG}	-65 to +150	°C

Table 4 –Absolute Maximum Ratings**7.2. Recommended DC Operating Conditions**

Parameter	Symbol	Min	Typical	Max	Unit
Supply voltage	V _{DD}	4.5	—	5.5	V
Case temperature range	T _C	-55	—	+125	°C
High-level input voltage	V _{IH}	2.4	—	—	V
Low-level input voltage	V _{IL}	—	—	0.8	V

Table 5 - Recommended DC Operating Conditions**7.3. DC CHARACTERISTICS**

Symbol	Parameter	Condition	Min	Typical	Max	Unit
V _{OL}	Output voltage low level	I _{OL} = 4.0mA, V _{DD} = 4.5V (TTL)	—	-	0.4	V
V _{OH}	Output voltage high level	I _{OH} = -2.0mA, V _{DD} = 4.5V (TTL)	2.4	-	—	V
I _{DD1} (OP)	Supply current operating @25.0MHz (40ns product) @22.2MHz (45ns product)	TTL inputs levels (I _{OUT} = 0), V _{IL} = 0.2V V _{DD} , #PE = 5.5V	—	-	125 117	mA mA
I _{DD2} (SB)	Supply current standby	CMOS input levels V _{IL} = V _{SS} +0.25V CE = V _{DD} - 0.25 V _{IH} = V _{DD} - 0.25V	—	-	2	mA

Table 6 - DC Characteristics**8. READ CYCLE**

A combination of #PE greater than V_{IH}(min), and #CE less than V_{IL}(max) defines a read cycle. Read access time is measured from the latter of device enable, output enable, or valid address to valid data output.

An address access read is initiated by a change in address inputs while the chip is enabled with #OE asserted and #PE deasserted. Valid data appears on data output, DQ(7:0), after the specified t_{AVQV} is satisfied. Outputs remain active throughout the entire cycle. As long as device enable and output enable are active, the address inputs may change at a rate equal to the minimum read cycle time.

8.1. AC CHARACTERISTICS

(V_{DD} = 5.0V ±10%; -55°C < T_C < +125°C)

Symbol	Parameter	Min	Max	Unit
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t_{AVAV}	Read cycle time	45	—	ns
t_{AVQV}	Read access time	—	45	ns
t_{AXQX}	Output hold time	0	—	ns
t_{GLQX}	#OE-controlled output enable time	0	—	ns
t_{GLQV}	#OE-controlled access time	—	15	ns
t_{GHQZ}	#OE-controlled output three-state time	—	15	ns
t_{ELQX}	#CE-controlled output enable time	0	—	ns
t_{ELQV}	#CE-controlled access time	—	45	ns
t_{EHQZ}	#CE-controlled output three-state time	—	15	ns

Table 7 - AC Characteristics

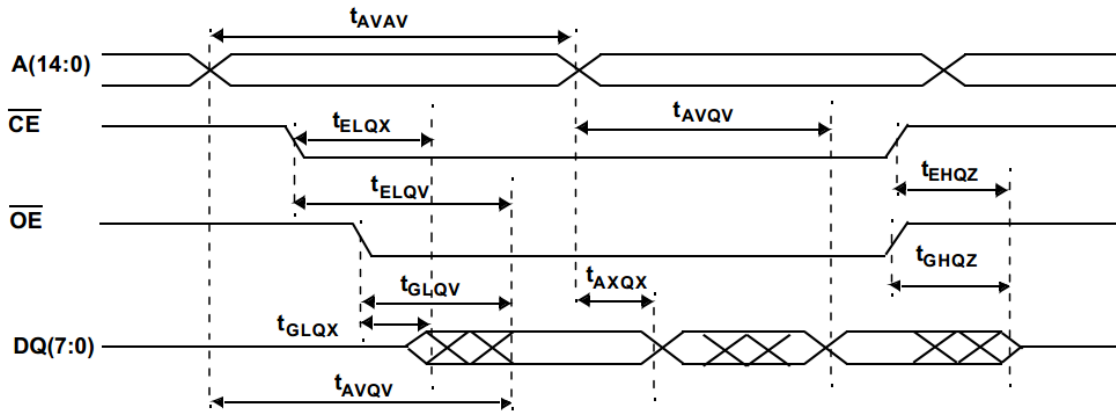


Figure 2-PROM Read Cycle

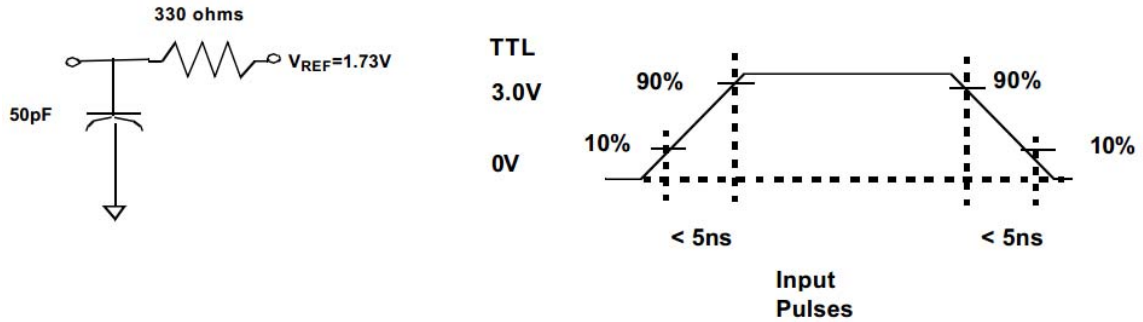
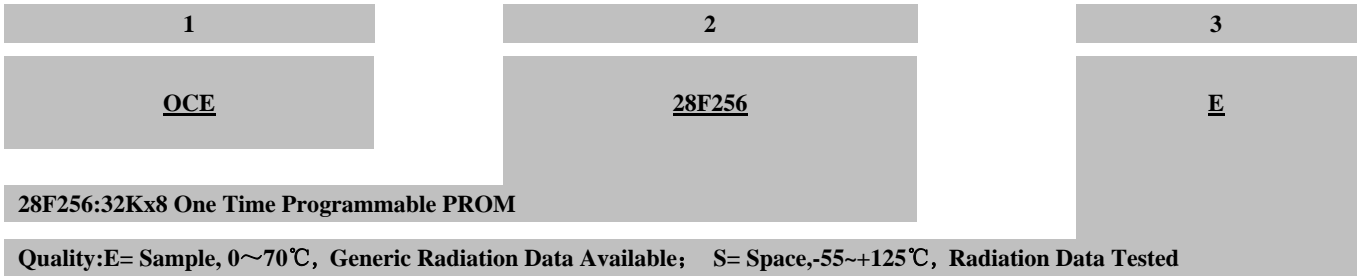


Figure 3-AC Test Loads and Input Waveforms

9. ORDERING INFORMATION

Part numbering:



Part Number	Capacity (bit)	Radiation			Bus Width (bit)	Temp range (°C)	Quality Flow
		TID ³	SEL ⁴	SEU ⁵			
OCE28F256E	256k	-	-	-	8	0~+70	Sample
OCE28F256S	256k	1E5	>75	37.3	8	-55~+125	Space

Table 8 –Part numbers

10. PACKAGE TYPE AND DIMENSIONS

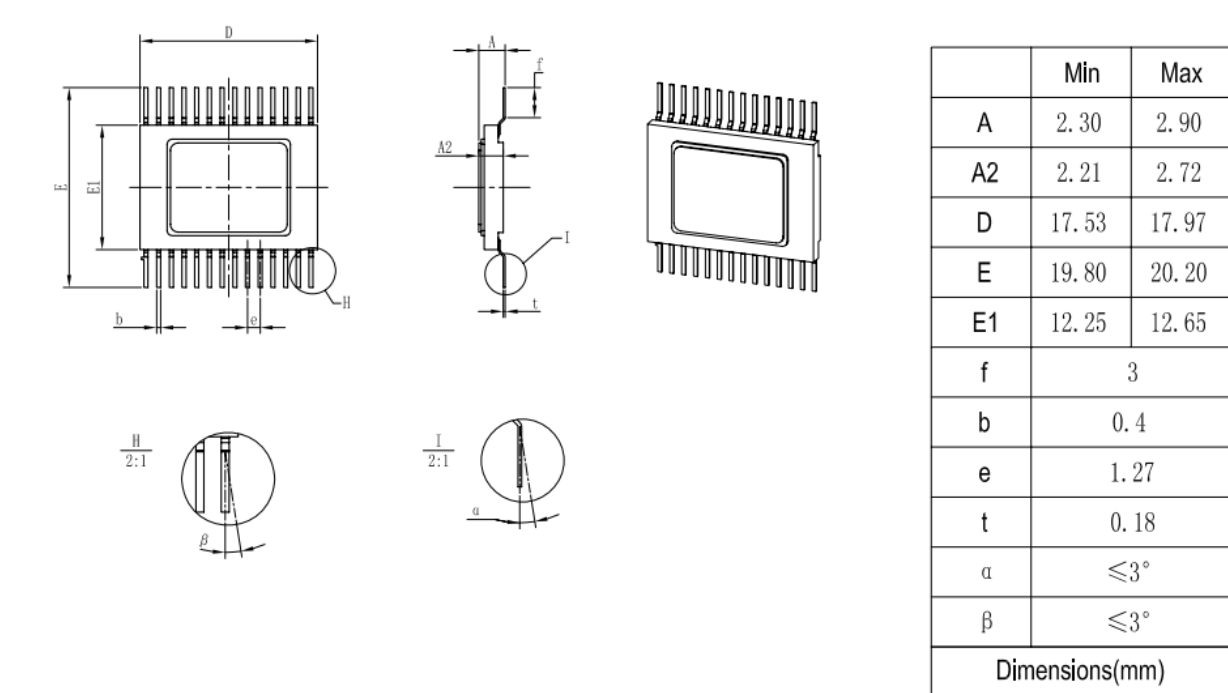


Figure 4–Mechanical outlines

³ TID: Total Dose (Krads(Si))
⁴ SEL:LET Threshold (Mev.cm2/mg)
⁵ SEU:SEU Threshold (Mev.cm2/mg)

11. REVISIONHISTORY

Revision	Date	Description of Change
A0	Mar,13,2018	First created.

Table 9 –Revision history